FIG. 1

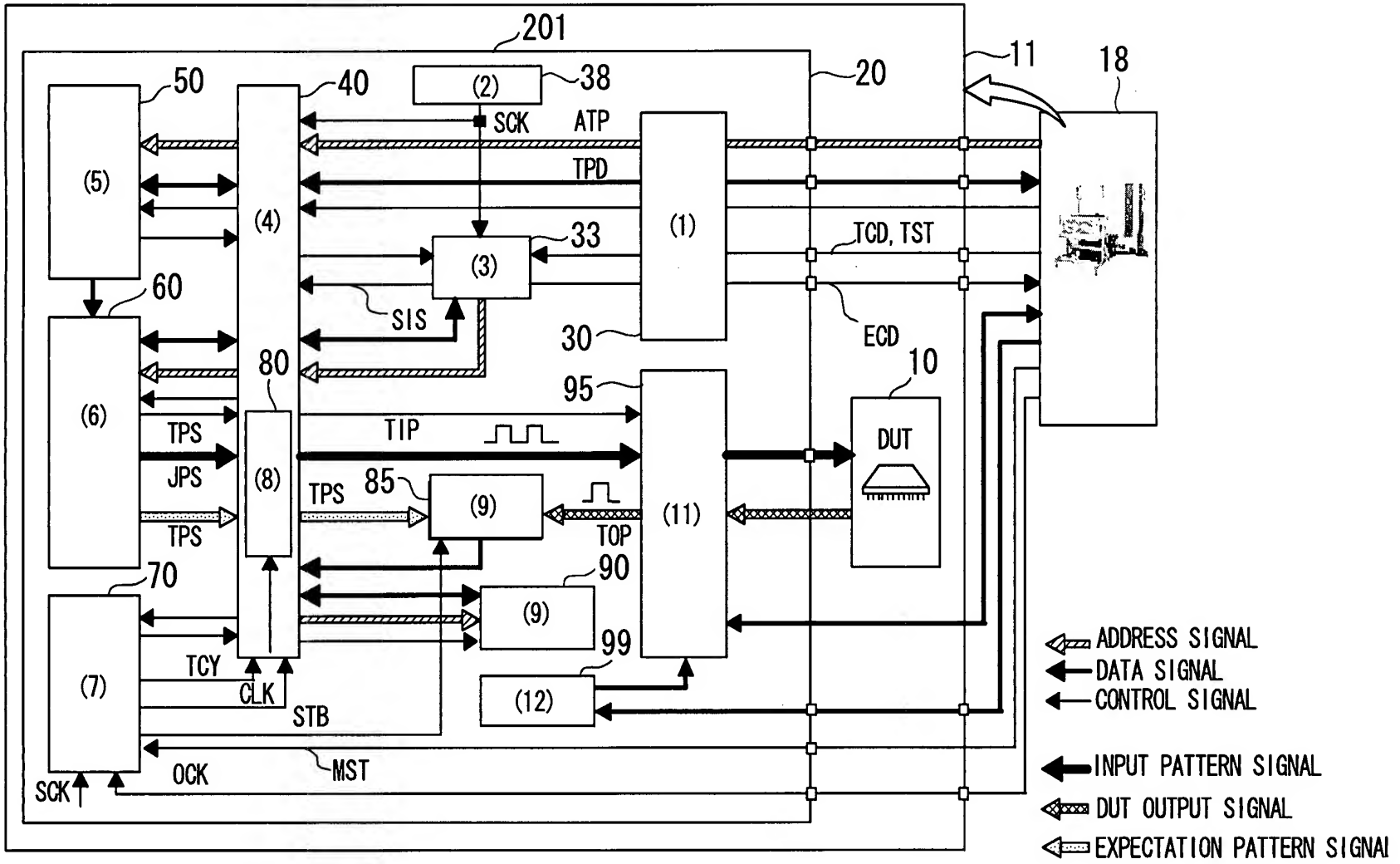

201
11
18
20
50
40
(2)
38
SCK
ATP
TPD
(5)
(4)
(1)
33
(3)
TCD, TST
60
SIS
ECD
30
80
95
10
(6)
TPS
TIP
DUT
JPS
(8)
TPS
85
(9)
(11)
TPS
TOP
70
90
(9)
99
(7)
TCY
CLK
STB
(12)
OCK
MST
SCK
ADDRESS SIGNAL
DATA SIGNAL
CONTROL SIGNAL
INPUT PATTERN SIGNAL
DUT OUTPUT SIGNAL
EXPECTATION PATTERN SIGNAL

FIG. 2

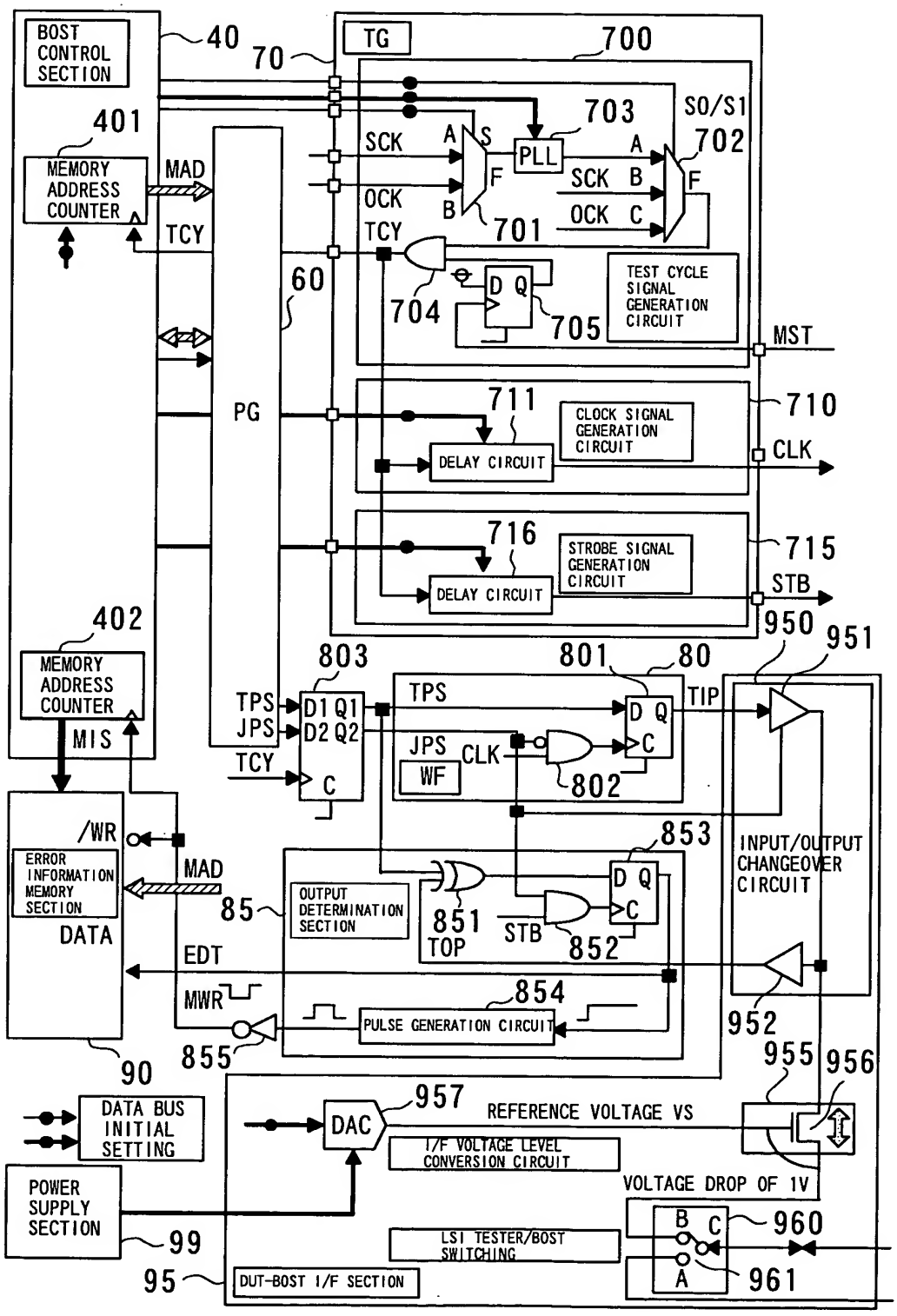

BOST CONTROL SECTION
40
70
TG
700
401
MEMORY ADDRESS COUNTER
MAD
TCY
SCK
OCK
A
B
S
F
703
PLL
SO/S1
702
701
TEST CYCLE SIGNAL GENERATION CIRCUIT
704
705
60
MST
PG
711
CLOCK SIGNAL GENERATION CIRCUIT
710
DELAY CIRCUIT
CLK
716
STROBE SIGNAL GENERATION CIRCUIT
715
STB
402
MEMORY ADDRESS COUNTER
MIS
803
801
80
950
951
TPS
JPS
D1 Q1
D2 Q2
C
D Q
TIP
WF
CLK
802
/WR
ERROR INFORMATION MEMORY SECTION
DATA
853
INPUT/OUTPUT CHANGEOVER CIRCUIT
85
OUTPUT DETERMINATION SECTION
851
TOP
852
EDT
MWR
854
PULSE GENERATION CIRCUIT
952
855
90
955
956
DATA BUS INITIAL SETTING
957
DAC
REFERENCE VOLTAGE VS
I/F VOLTAGE LEVEL CONVERSION CIRCUIT
VOLTAGE DROP OF 1V
POWER SUPPLY SECTION
99
LSI TESTER/BOST SWITCHING
960
961
95
DUT-BOST I/F SECTION

FIG. 3

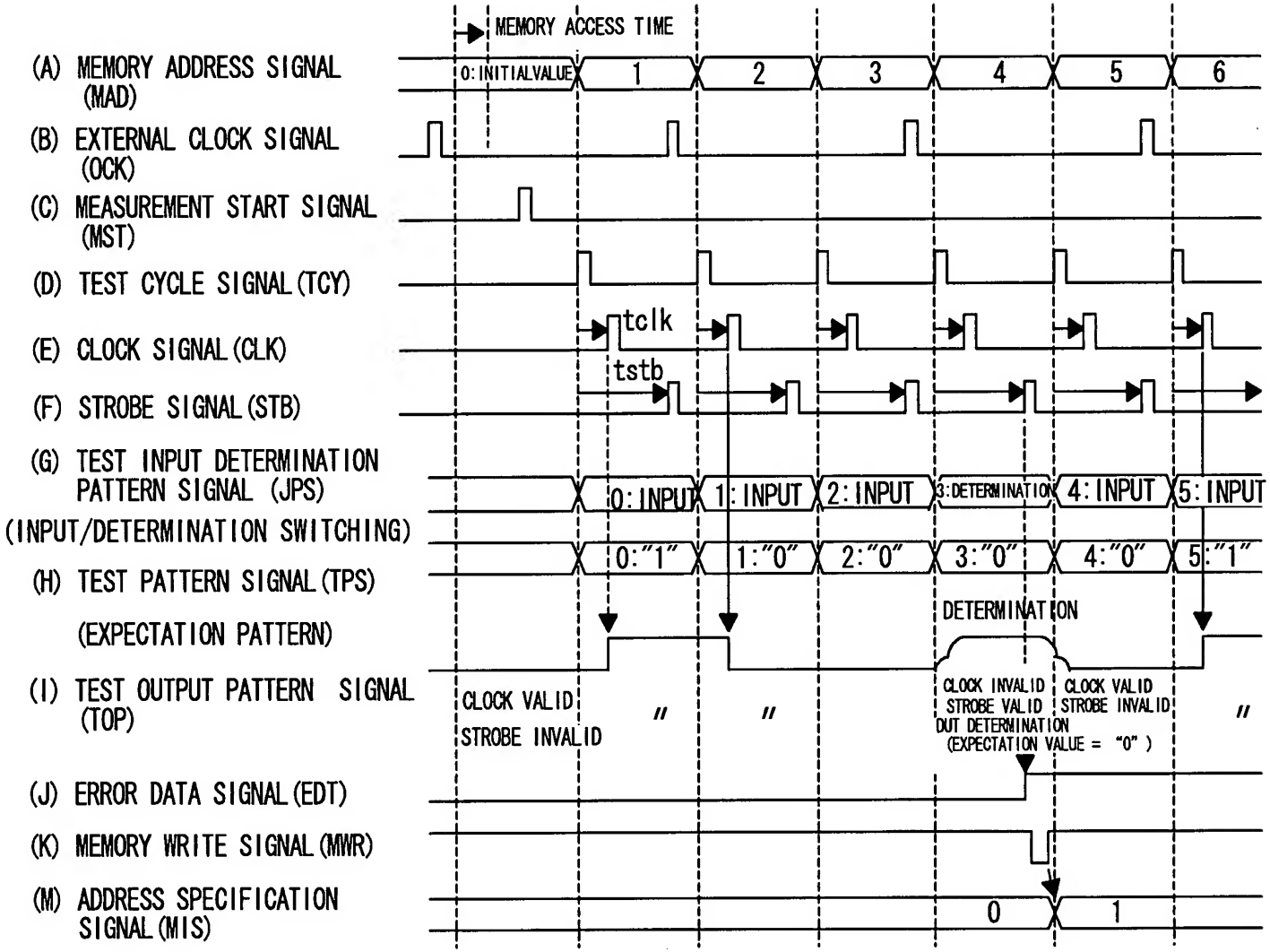

MEMORY ACCESS TIME
(A) MEMORY ADDRESS SIGNAL (MAD)
0: INITIALVALUE
1
2
3
4
5
6
(B) EXTERNAL CLOCK SIGNAL (OCK)
(C) MEASUREMENT START SIGNAL (MST)
(D) TEST CYCLE SIGNAL (TCY)
tclk
(E) CLOCK SIGNAL (CLK)
tstb
(F) STROBE SIGNAL (STB)
(G) TEST INPUT DETERMINATION PATTERN SIGNAL (JPS)
0: INPUT
1: INPUT
2: INPUT
3: DETERMINATION
4: INPUT
5: INPUT
(INPUT/DETERMINATION SWITCHING)
(H) TEST PATTERN SIGNAL (TPS)
0: "1"
1: "0"
2: "0"
3: "0"
4: "0"
5: "1"
(EXPECTATION PATTERN)
DETERMINATION
(I) TEST OUTPUT PATTERN SIGNAL (TOP)
CLOCK VALID
STROBE INVALID
CLOCK INVALID
STROBE VALID
DUT DETERMINATION
(EXPECTATION VALUE = "0")
CLOCK VALID
STROBE INVALID
(J) ERROR DATA SIGNAL (EDT)
(K) MEMORY WRITE SIGNAL (MWR)
(M) ADDRESS SPECIFICATION SIGNAL (MIS)
0
1

FIG. 4A

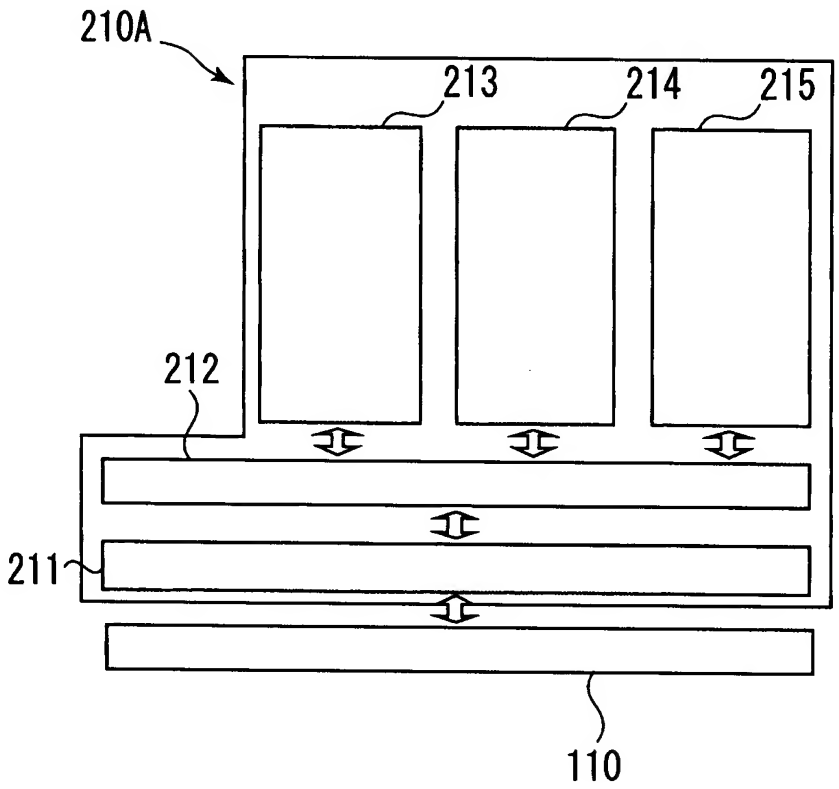


FIG. 4B

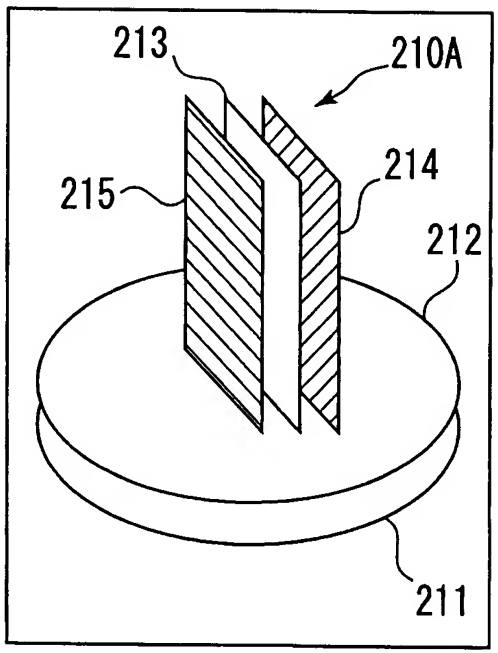


FIG. 5 A

FIG. 5 B

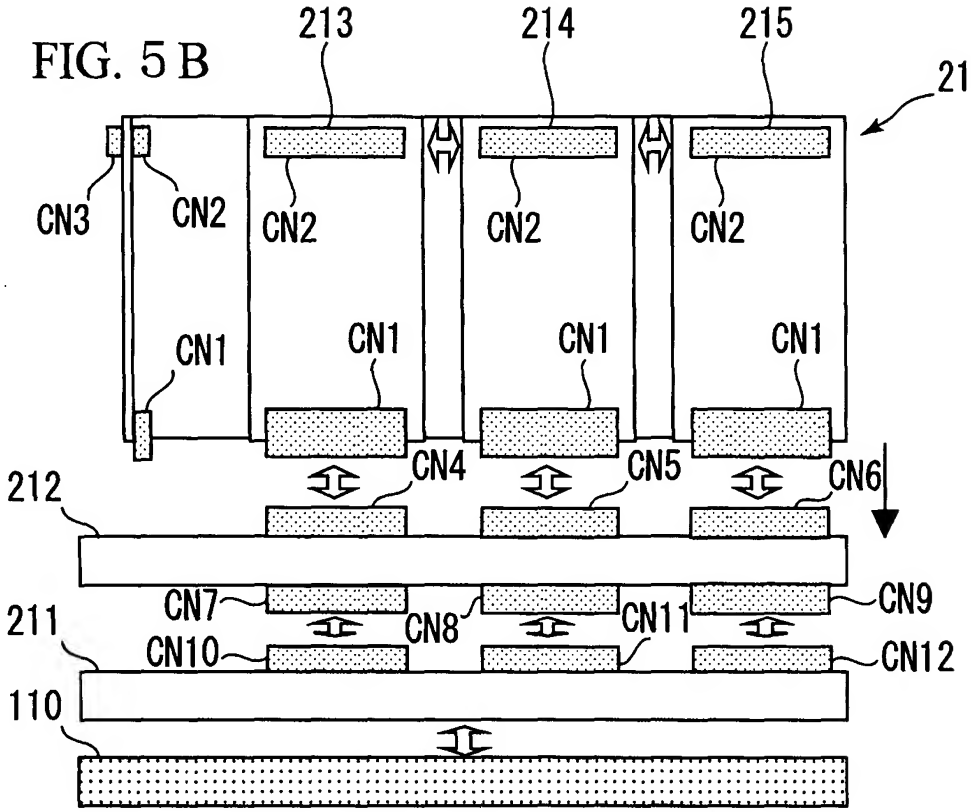


FIG. 5 C

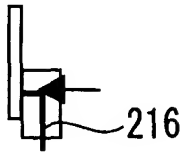


FIG. 6

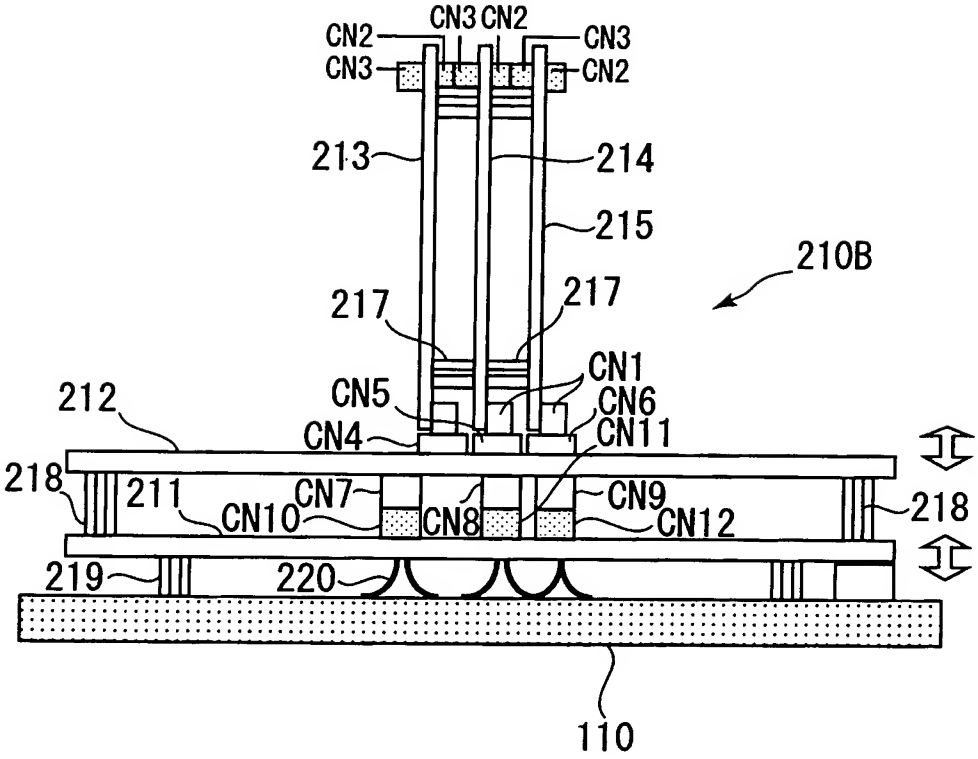

CN3 CN2
CN2
CN3
CN3
CN2
213
214
215
210B
217
217
CN1
CN5
CN6
212
CN4
CN11
218
211
CN7
CN9
218
CN10
CN8
CN12
219
220
110

FIG. 7A

FIG. 7B

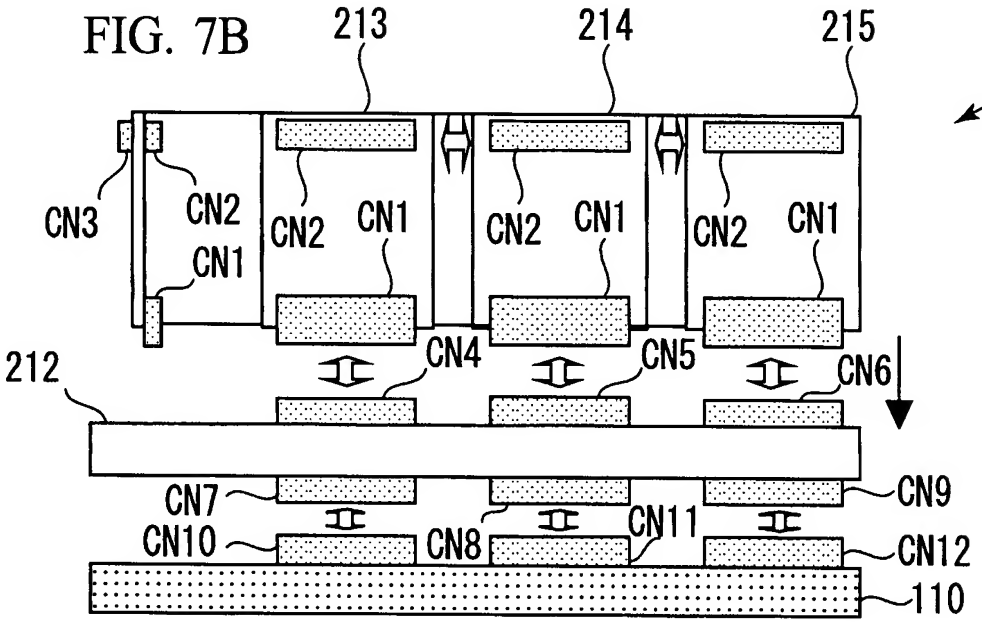


FIG. 7C

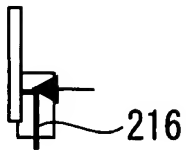


FIG. 8

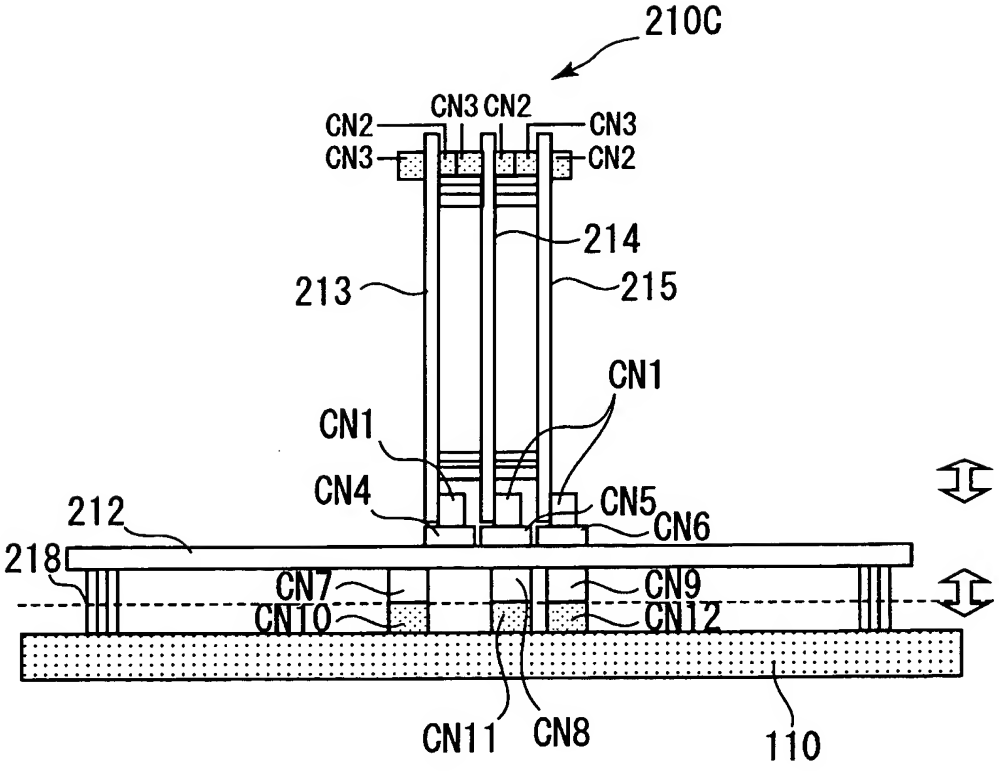

210C
CN3
CN2
CN2
CN3
CN3
CN2
214
213
215
CN1
CN1
CN4
CN5
CN6
212
218
CN7
CN9
CN10
CN12
CN11
CN8
110

FIG. 9A

FIG. 9B

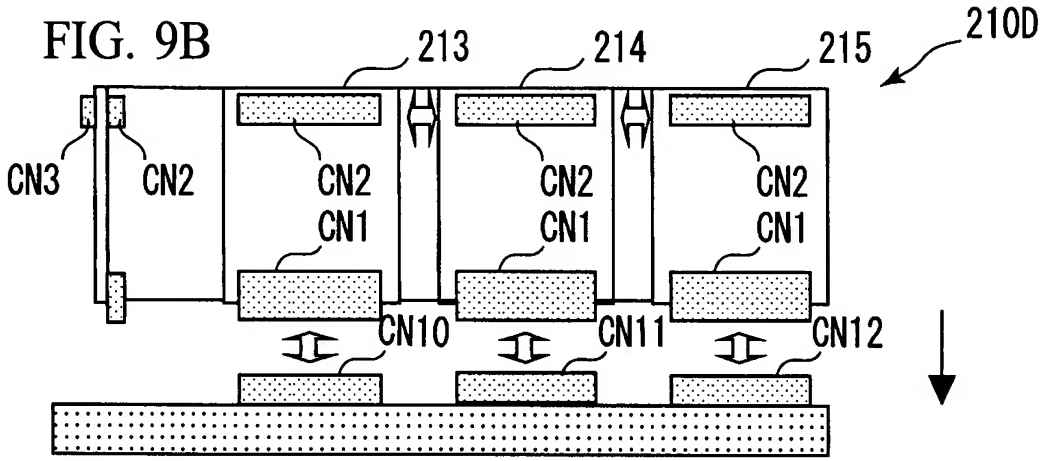


FIG. 9C

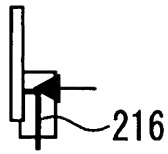


FIG. 10

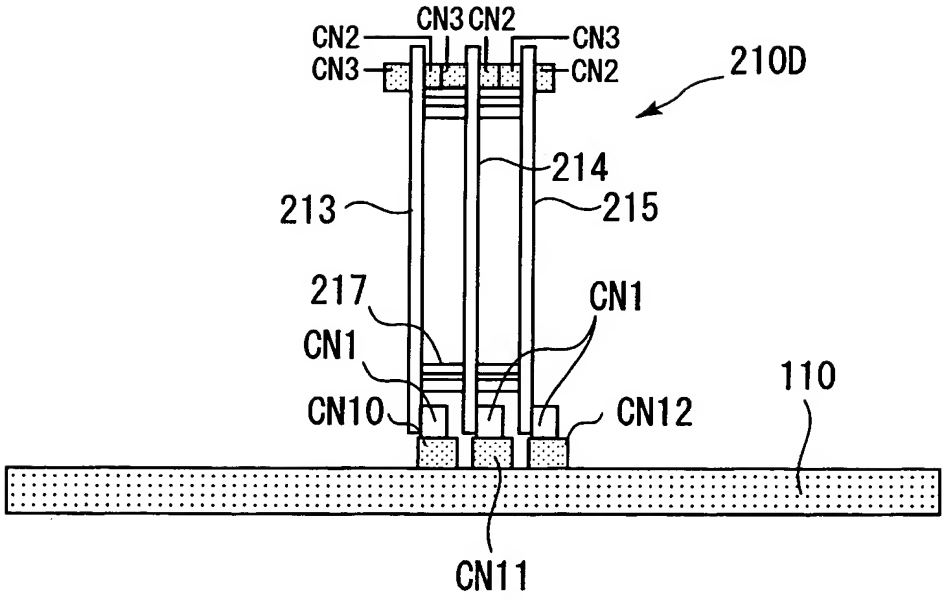

CN2
CN3
CN3
CN2
CN3
CN2
210D
214
213
215
217
CN1
CN1
110
CN10
CN12
CN11

FIG. 11A

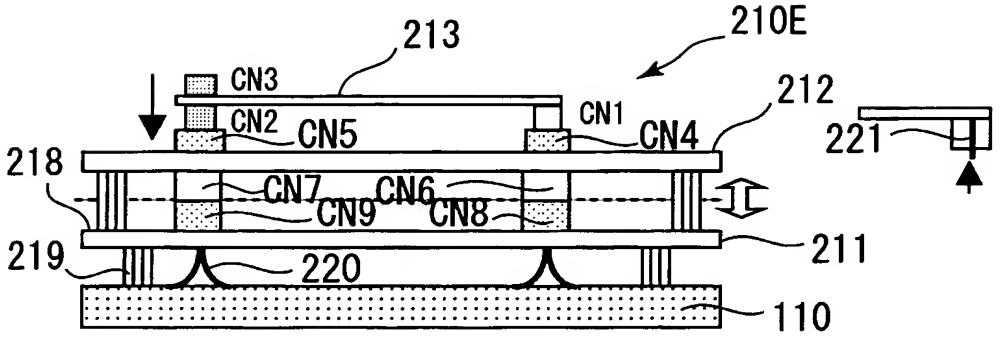


FIG. 11C

FIG. 11B

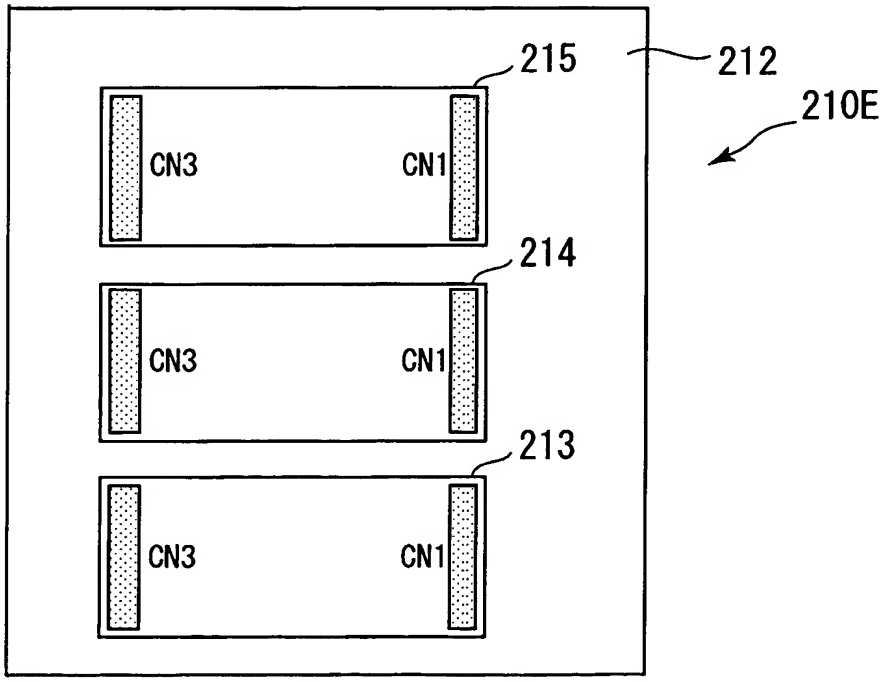


FIG. 12

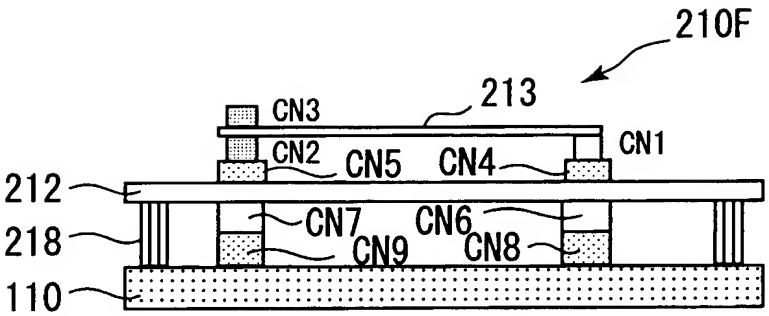

210F
213
CN3
CN1
CN2
CN5
CN4
212
CN7
CN6
218
CN9
CN8
110

FIG. 13

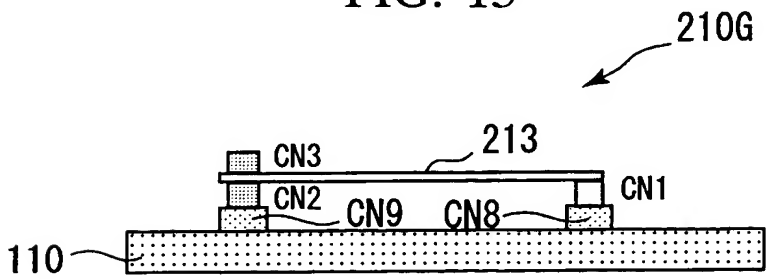

210G
213
CN3
CN1
CN2
CN9
CN8
110

FIG. 14A

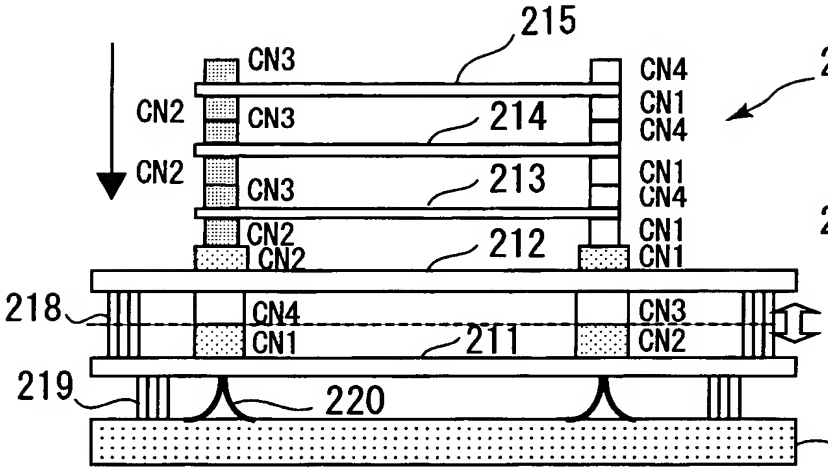


FIG. 14C

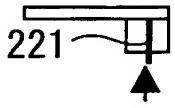


FIG. 14B

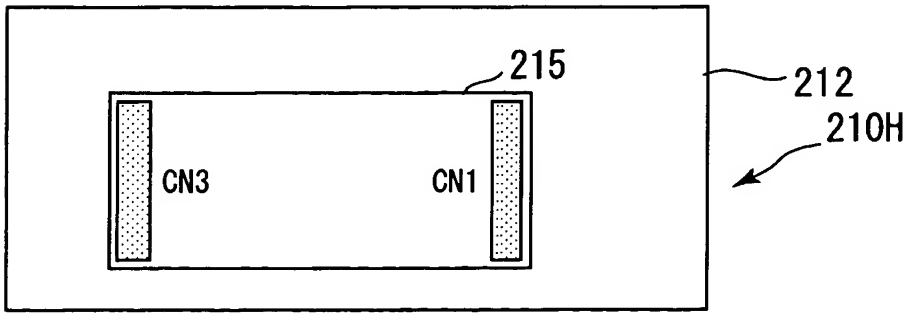


FIG. 15

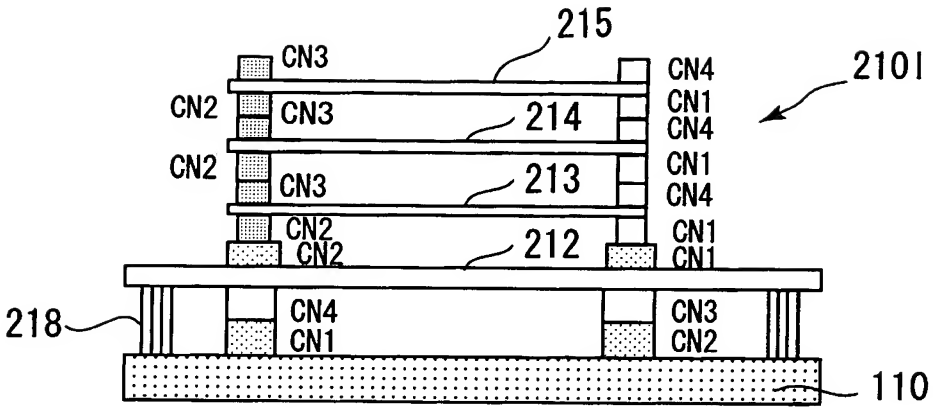

215
210I
CN3
CN4
CN2
CN3
214
CN1
CN4
CN2
CN3
213
CN1
CN4
CN2
CN2
212
CN1
CN1
218
CN4
CN1
CN3
CN2
110

FIG. 16

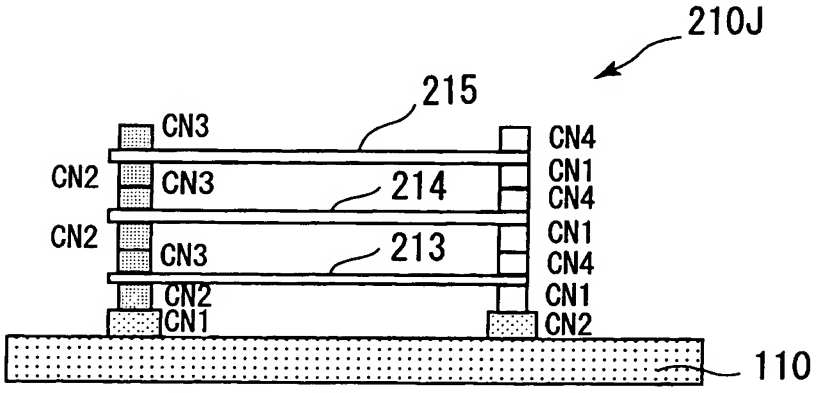

210J
215
CN3
CN4
CN2
CN3
214
CN1
CN4
CN2
CN3
213
CN1
CN4
CN2
CN1
CN1
CN2
110

FIG. 17

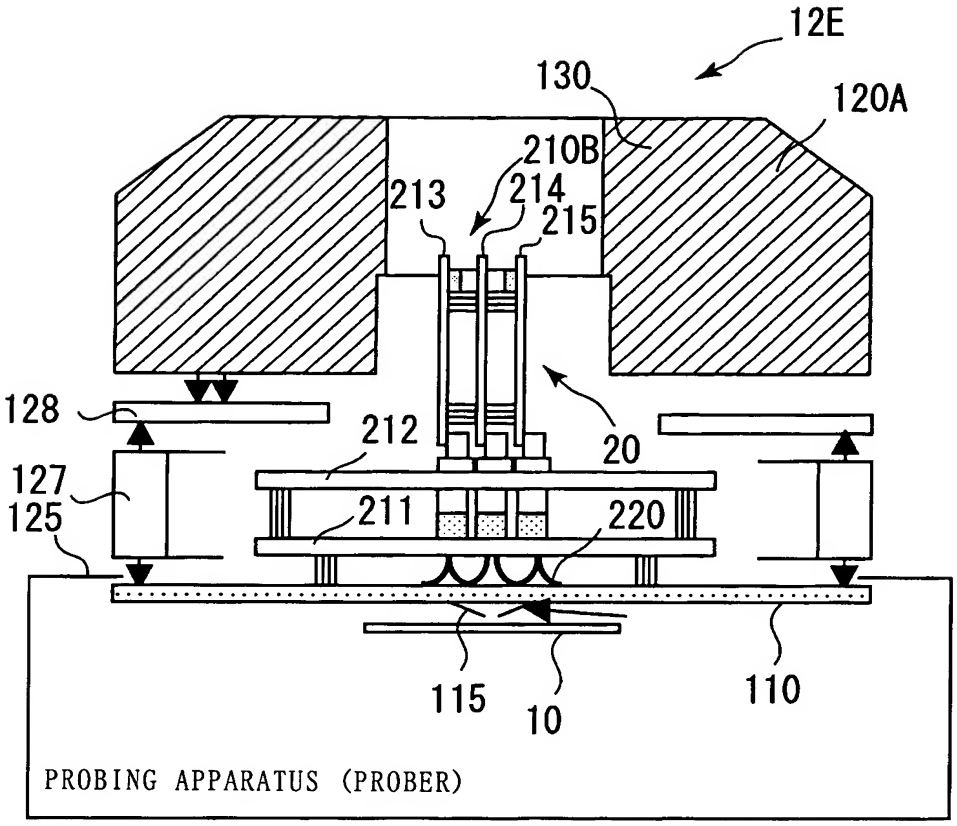

12E
130
120A
210B
213
214
215
128
212
20
127
125
211
220
115
10
110
PROBING APPARATUS (PROBER)

FIG. 18

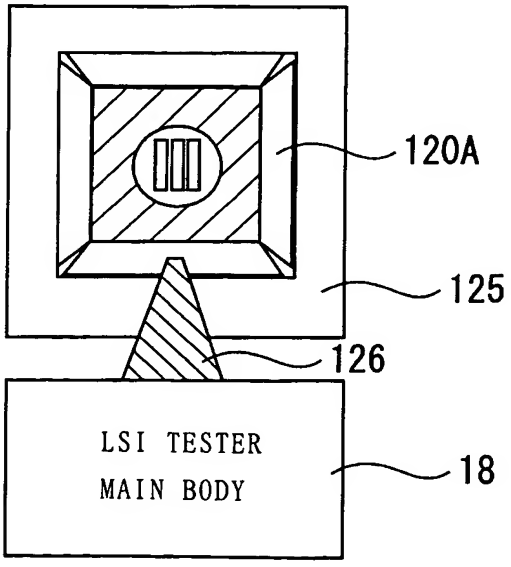

120A
125
126
LSI TESTER
MAIN BODY
18

FIG. 19

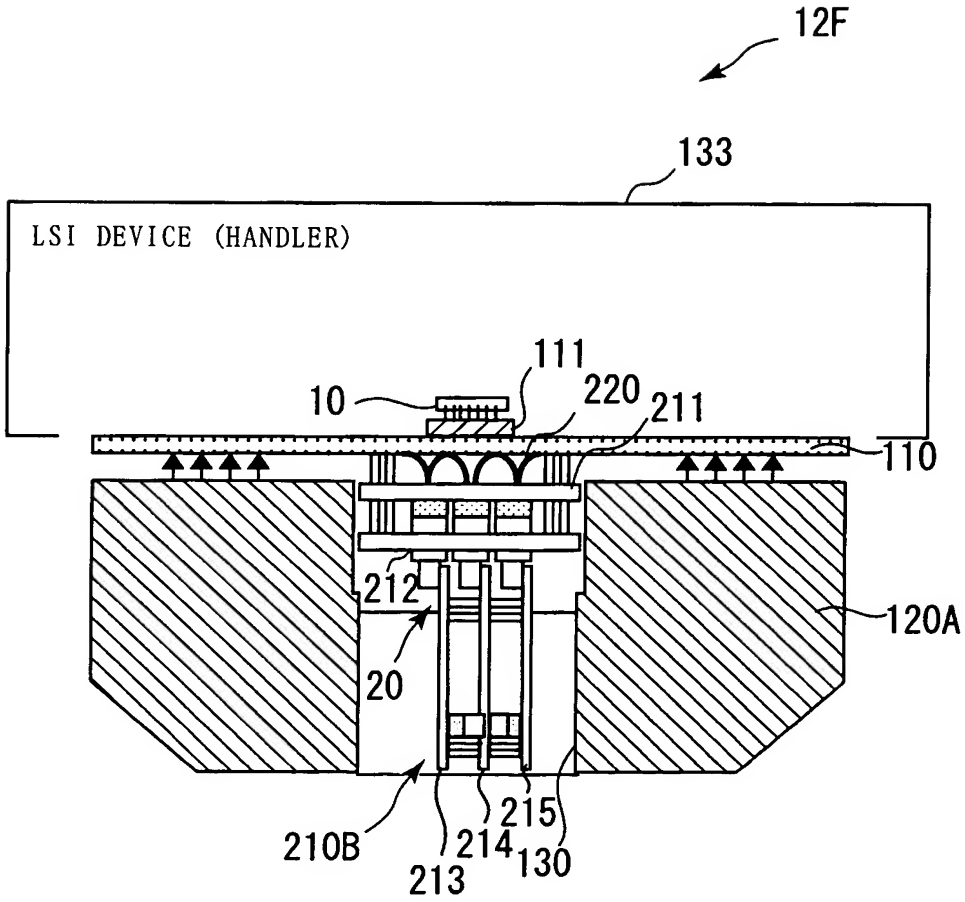

12F
133
LSI DEVICE (HANDLER)
111
10
220
211
110
212
120A
20
210B
213
214
215
130

FIG. 20A

FIG. 20B

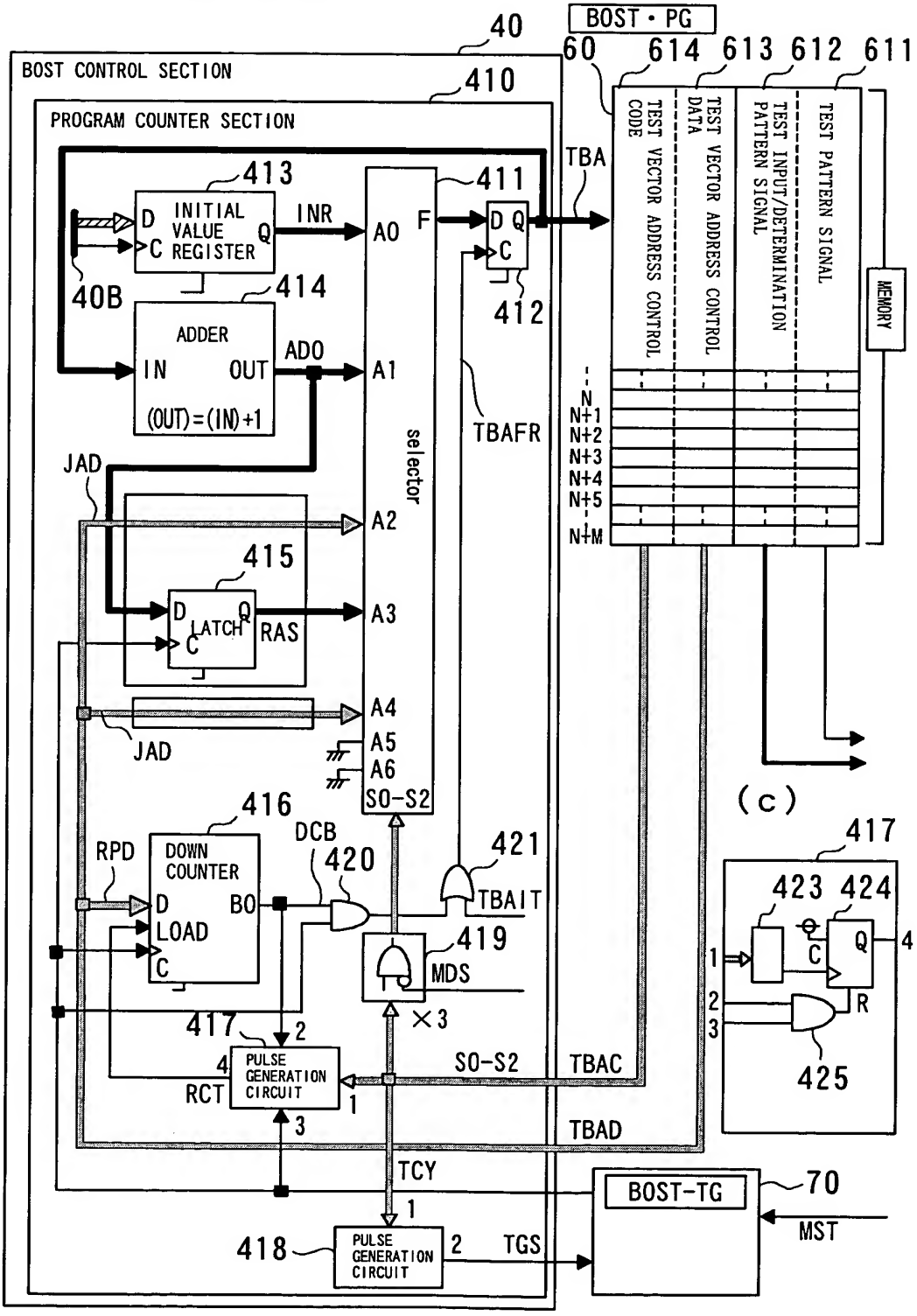


FIG. 21

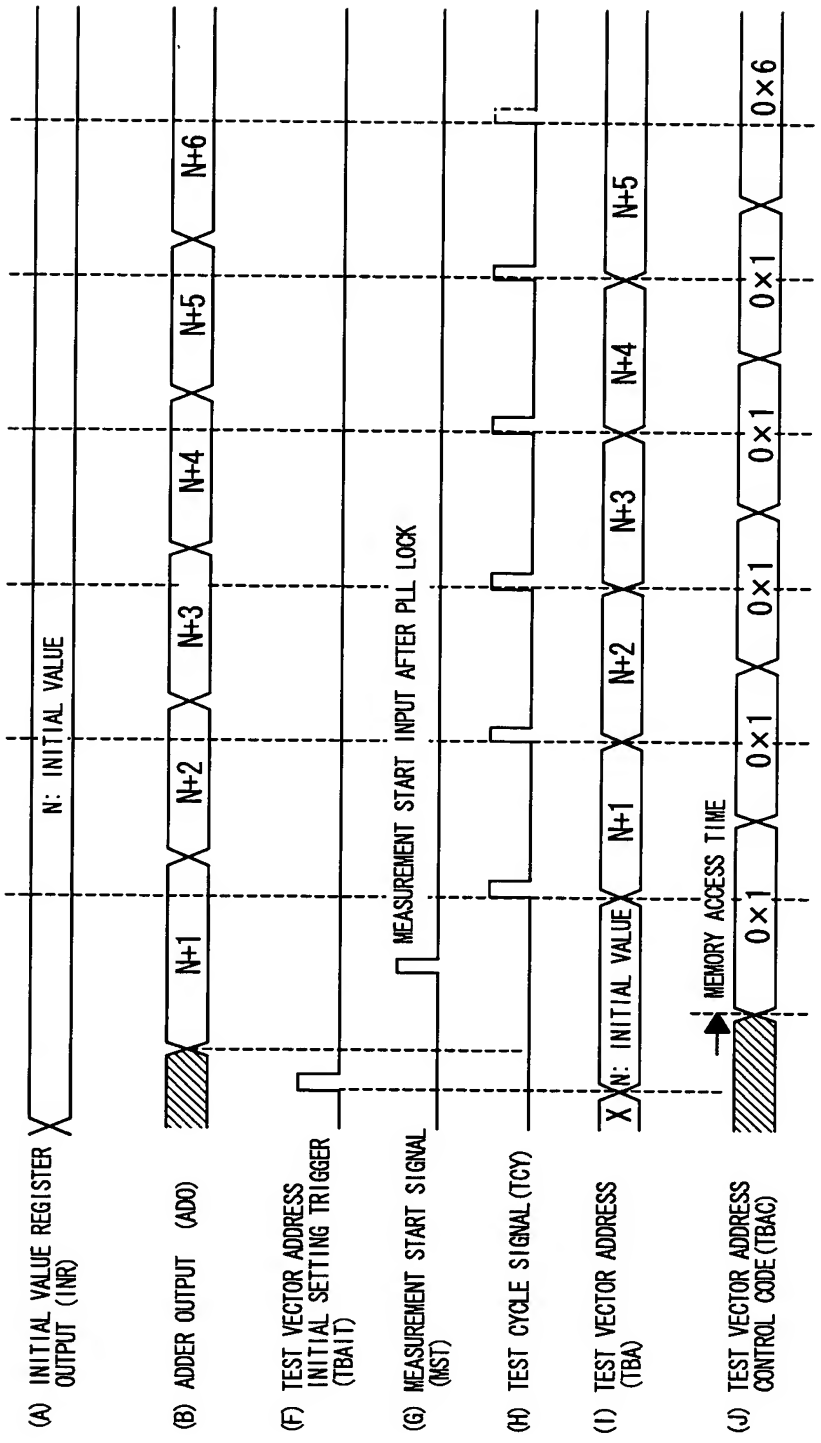

(A) INITIAL VALUE REGISTER OUTPUT (INR)
N: INITIAL VALUE
(B) ADDER OUTPUT (ADO)
N+1
N+2
N+3
N+4
N+5
N+6
(F) TEST VECTOR ADDRESS INITIAL SETTING TRIGGER (TBAIT)
(G) MEASUREMENT START SIGNAL (MST)
MEASUREMENT START INPUT AFTER PLL LOCK
(H) TEST CYCLE SIGNAL (TCY)
(I) TEST VECTOR ADDRESS (TBA)
X
N: INITIAL VALUE
N+1
N+2
N+3
N+4
N+5
MEMORY ACCESS TIME
(J) TEST VECTOR ADDRESS CONTROL CODE (TBAC)
0×1
0×1
0×1
0×1
0×1
0×6

FIG. 22

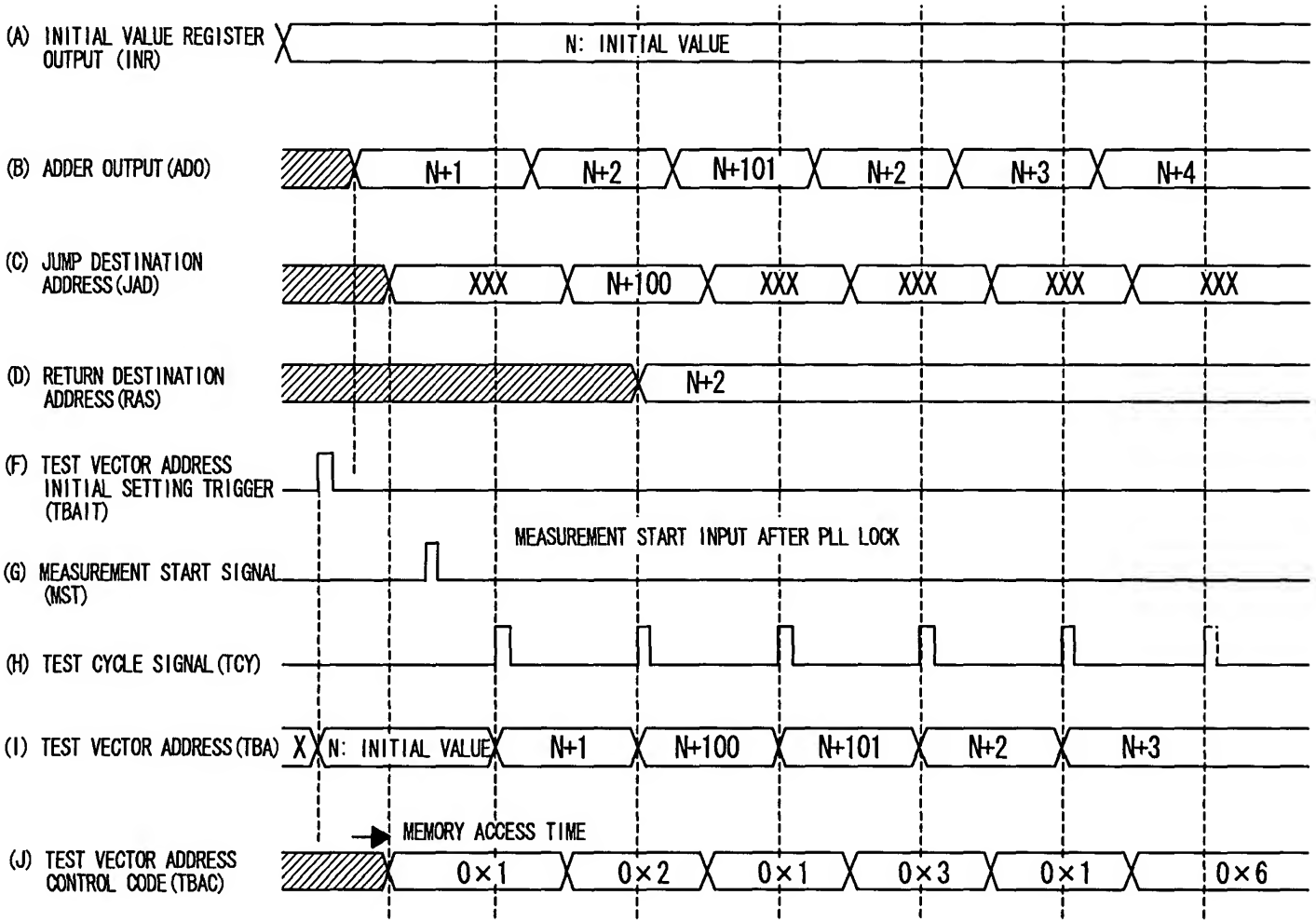

(A) INITIAL VALUE REGISTER OUTPUT (INR)
N: INITIAL VALUE
(B) ADDER OUTPUT (ADO)
N+1
N+2
N+101
N+2
N+3
N+4
(C) JUMP DESTINATION ADDRESS (JAD)
XXX
N+100
XXX
XXX
XXX
XXX
(D) RETURN DESTINATION ADDRESS (RAS)
N+2
(F) TEST VECTOR ADDRESS INITIAL SETTING TRIGGER (TBAIT)
MEASUREMENT START INPUT AFTER PLL LOCK
(G) MEASUREMENT START SIGNAL (MST)
(H) TEST CYCLE SIGNAL (TCY)
(I) TEST VECTOR ADDRESS (TBA)
N: INITIAL VALUE
N+1
N+100
N+101
N+2
N+3
MEMORY ACCESS TIME
(J) TEST VECTOR ADDRESS CONTROL CODE (TBAC)
0×1
0×2
0×1
0×3
0×1
0×6

FIG. 23

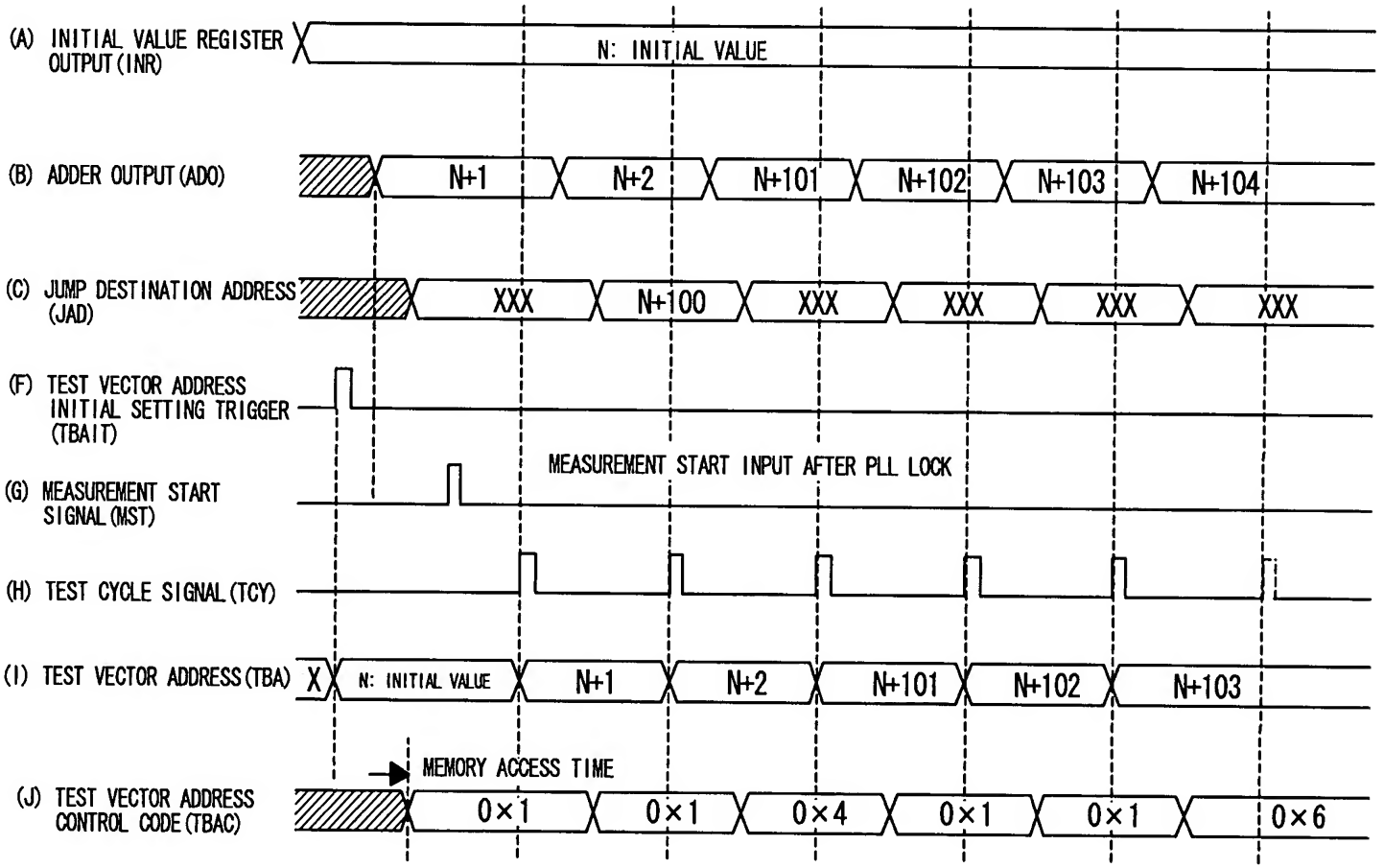

(A) INITIAL VALUE REGISTER OUTPUT (INR)
N: INITIAL VALUE
(B) ADDER OUTPUT (ADO)
N+1
N+2
N+101
N+102
N+103
N+104
(C) JUMP DESTINATION ADDRESS (JAD)
XXX
N+100
XXX
XXX
XXX
XXX
(F) TEST VECTOR ADDRESS INITIAL SETTING TRIGGER (TBAIT)
MEASUREMENT START INPUT AFTER PLL LOCK
(G) MEASUREMENT START SIGNAL (MST)
(H) TEST CYCLE SIGNAL (TCY)
(I) TEST VECTOR ADDRESS (TBA)
X
N: INITIAL VALUE
N+1
N+2
N+101
N+102
N+103
MEMORY ACCESS TIME
(J) TEST VECTOR ADDRESS CONTROL CODE (TBAC)
0×1
0×1
0×4
0×1
0×1
0×6

FIG. 24

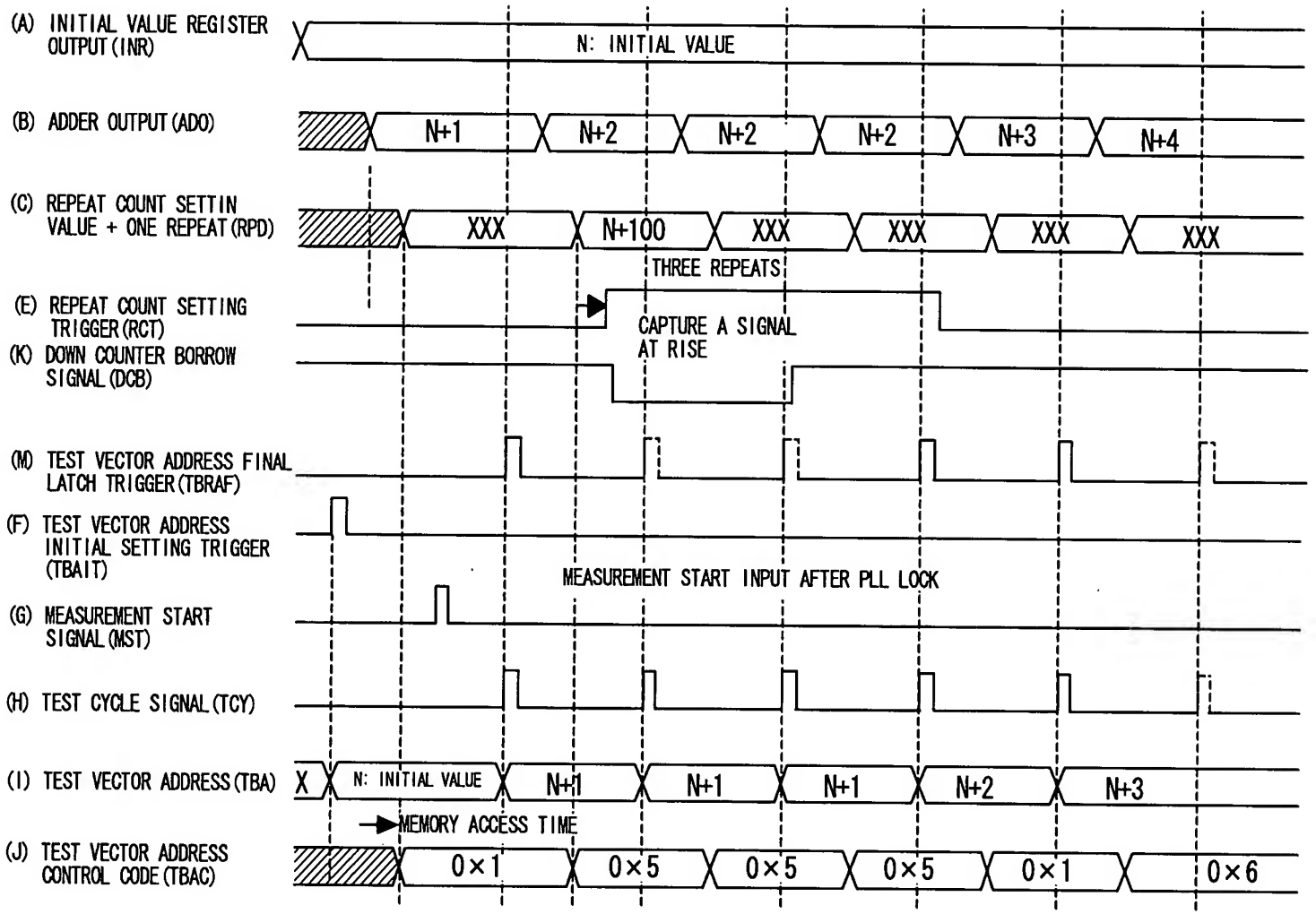

(A) INITIAL VALUE REGISTER OUTPUT (INR)
N: INITIAL VALUE
(B) ADDER OUTPUT (ADO)
N+1
N+2
N+2
N+2
N+3
N+4
(C) REPEAT COUNT SETTIN VALUE + ONE REPEAT (RPD)
XXX
N+100
XXX
XXX
XXX
XXX
THREE REPEATS
(E) REPEAT COUNT SETTING TRIGGER (RCT)
CAPTURE A SIGNAL AT RISE
(K) DOWN COUNTER BORROW SIGNAL (DCB)
(M) TEST VECTOR ADDRESS FINAL LATCH TRIGGER (TBRAF)
(F) TEST VECTOR ADDRESS INITIAL SETTING TRIGGER (TBAIT)
MEASUREMENT START INPUT AFTER PLL LOCK
(G) MEASUREMENT START SIGNAL (MST)
(H) TEST CYCLE SIGNAL (TCY)
(I) TEST VECTOR ADDRESS (TBA)
X
N: INITIAL VALUE
N+1
N+1
N+1
N+2
N+3
MEMORY ACCESS TIME
(J) TEST VECTOR ADDRESS CONTROL CODE (TBAC)
0×1
0×5
0×5
0×5
0×1
0×6

FIG. 25B

FIG. 25A

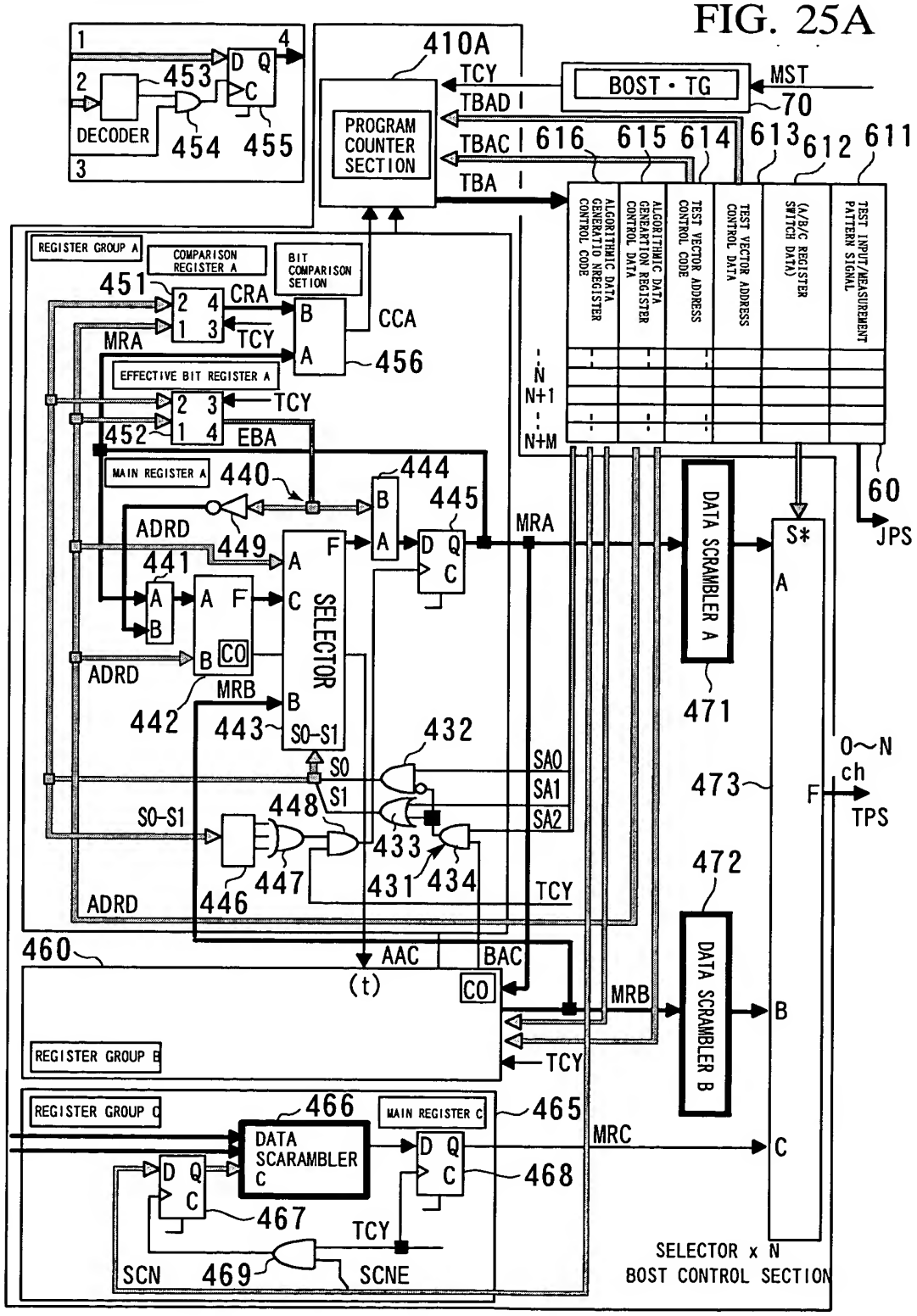


FIG. 26A

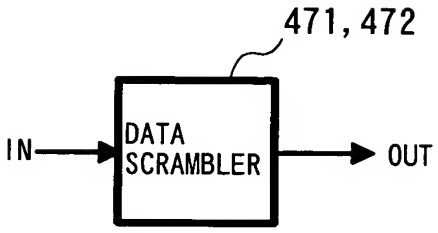


FIG. 26B

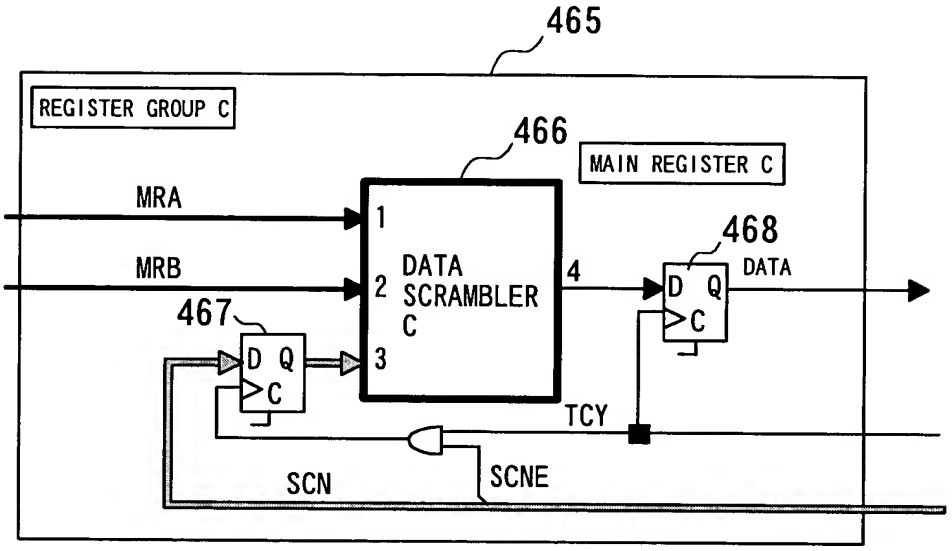


FIG. 26C

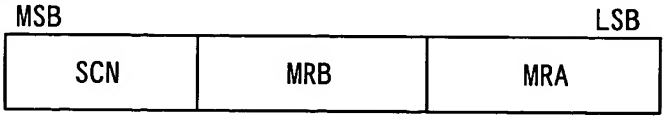


FIG. 27

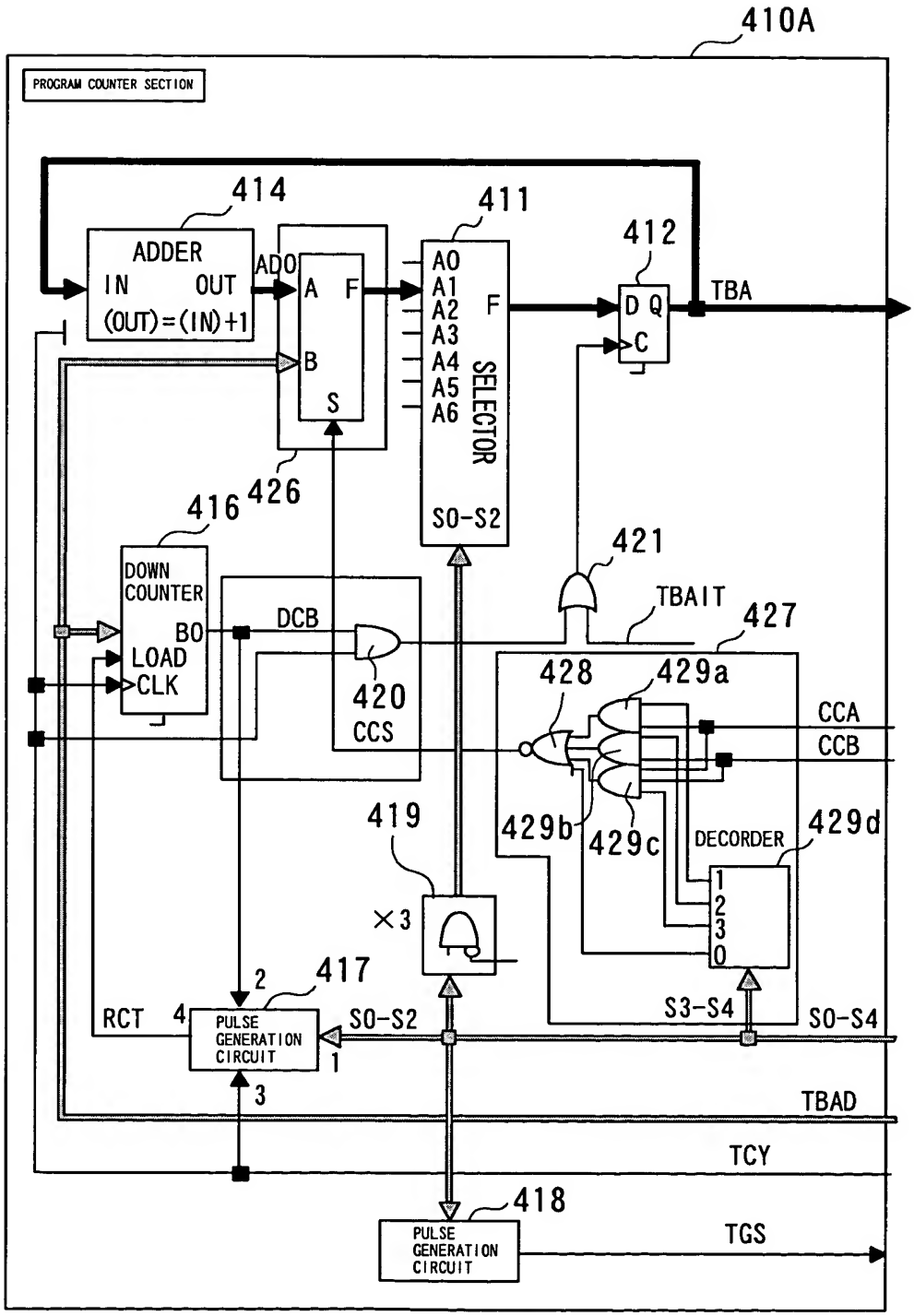

410A
PROGRAM COUNTER SECTION
414
ADDER
IN OUT
(OUT)=(IN)+1
ADO
A F
B
S
426
411
A0
A1
A2
A3
A4
A5
A6
F
SELECTOR
S0-S2
412
D Q
C
TBA
416
DOWN COUNTER
BO
LOAD
CLK
DCB
420
CCS
421
TBAIT
427
428
429a
429b
429c
CCA
CCB
DECORDER
429d
1
2
3
0
419
×3
2
417
RCT
4
PULSE GENERATION CIRCUIT
1
3
S0-S2
S3-S4
S0-S4
TBAD
TCY
418
PULSE GENERATION CIRCUIT
TGS

FIG. 28

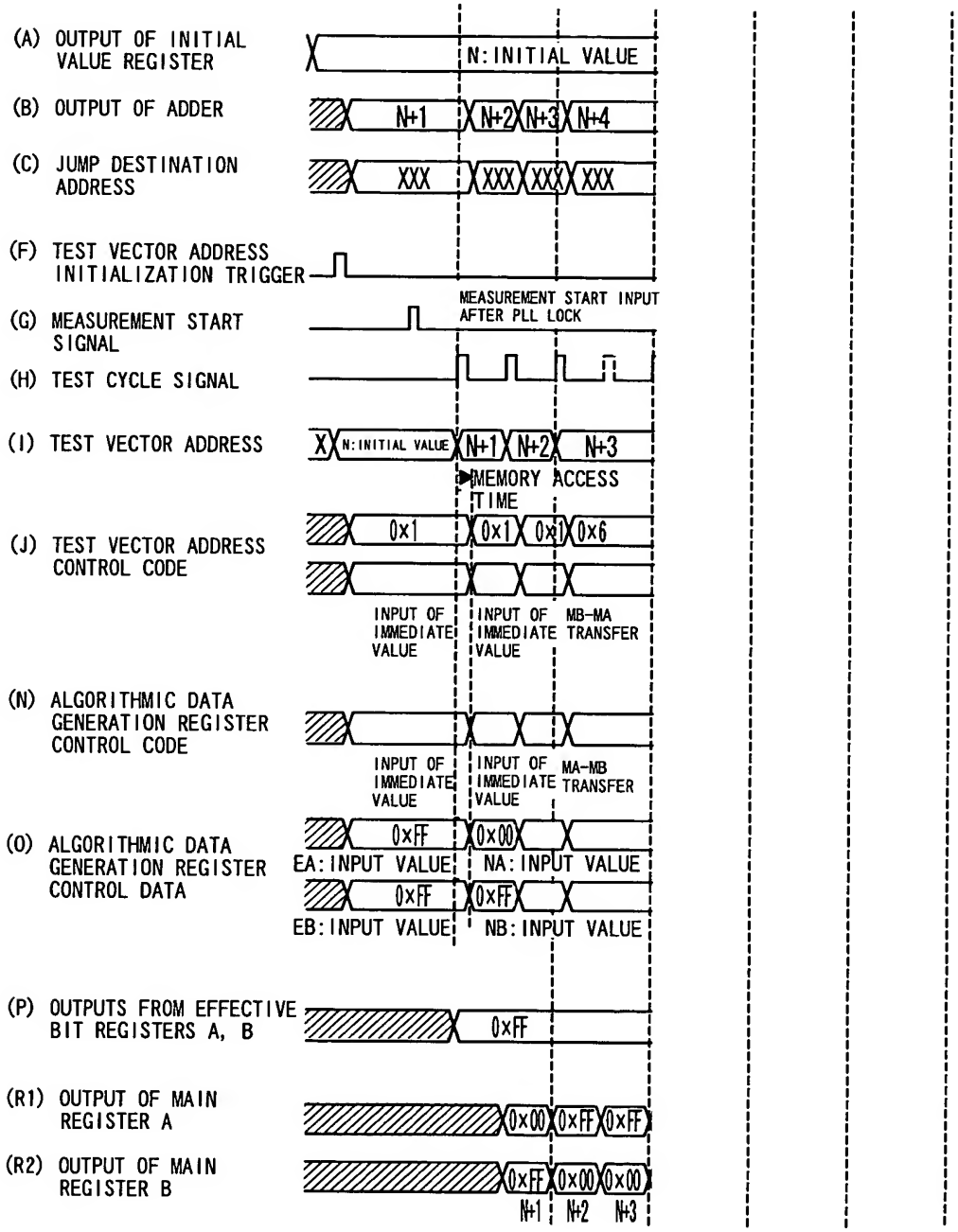

(A) OUTPUT OF INITIAL VALUE REGISTER
N: INITIAL VALUE
(B) OUTPUT OF ADDER
N+1
N+2
N+3
N+4
(C) JUMP DESTINATION ADDRESS
XXX
(F) TEST VECTOR ADDRESS INITIALIZATION TRIGGER
MEASUREMENT START INPUT AFTER PLL LOCK
(G) MEASUREMENT START SIGNAL
(H) TEST CYCLE SIGNAL
(I) TEST VECTOR ADDRESS
MEMORY ACCESS TIME
(J) TEST VECTOR ADDRESS CONTROL CODE
0x1
0x6
INPUT OF IMMEDIATE VALUE
MB-MA TRANSFER
(N) ALGORITHMIC DATA GENERATION REGISTER CONTROL CODE
MA-MB TRANSFER
(O) ALGORITHMIC DATA GENERATION REGISTER CONTROL DATA
0xFF
0x00
EA: INPUT VALUE
NA: INPUT VALUE
EB: INPUT VALUE
NB: INPUT VALUE
(P) OUTPUTS FROM EFFECTIVE BIT REGISTERS A, B
(R1) OUTPUT OF MAIN REGISTER A
(R2) OUTPUT OF MAIN REGISTER B

FIG. 29

	TBA	TBAC CODE OUTPUT	ADRC
↓	N	NOP (0x1)	EA=0xFF EB=0xFF
	N+1	NOP (0x1)	MA=0x00 MB=0xFF
	N+2	NOP (0x1)	MA=MB MB=MA
	N+3	STOP (0x6)	

FIG. 30

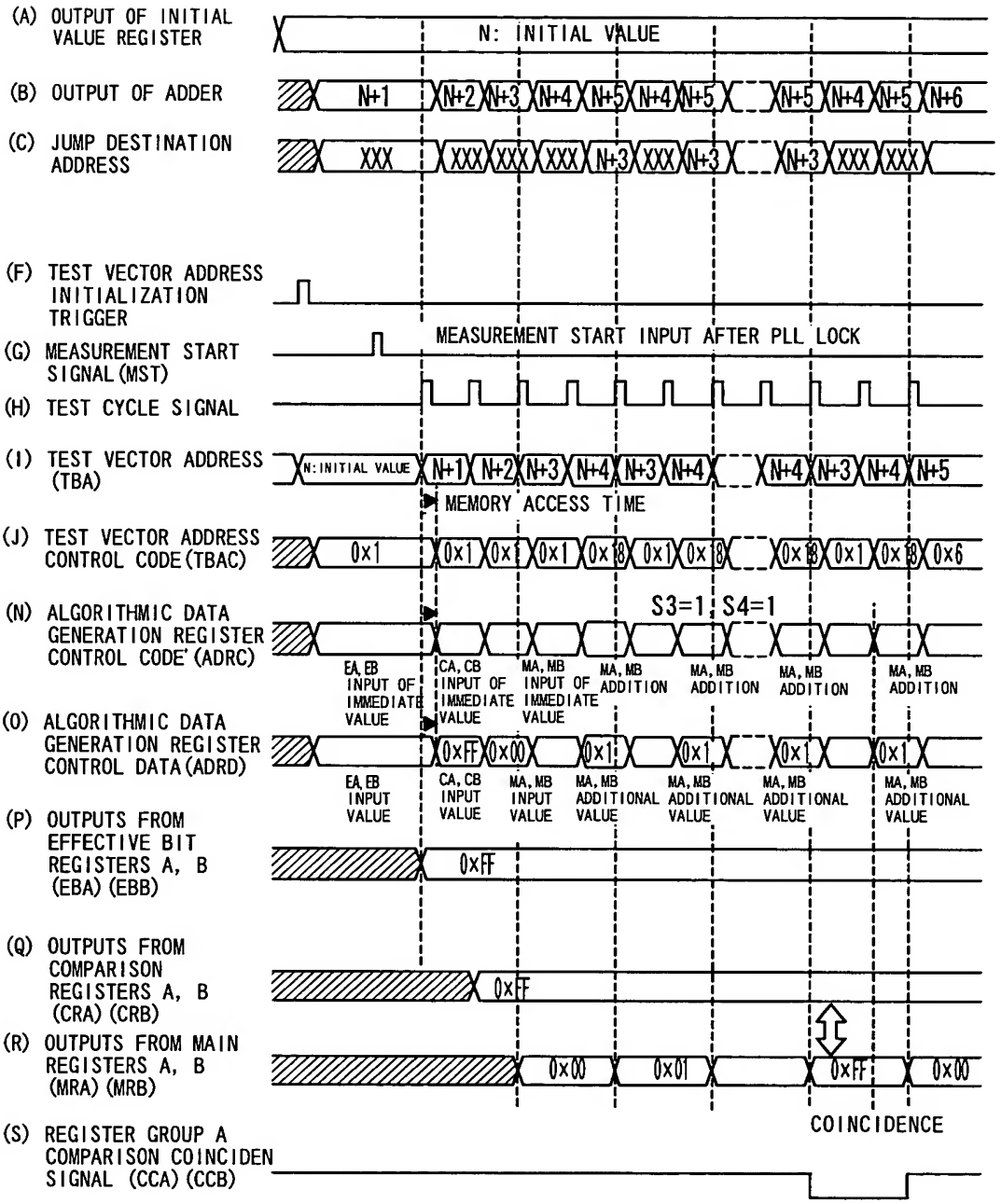

(A) OUTPUT OF INITIAL VALUE REGISTER
N: INITIAL VALUE
(B) OUTPUT OF ADDER
N+1 N+2 N+3 N+4 N+5 N+4 N+5 N+5 N+4 N+5 N+6
(C) JUMP DESTINATION ADDRESS
XXX XXX XXX XXX N+3 XXX N+3 N+3 XXX XXX
(F) TEST VECTOR ADDRESS INITIALIZATION TRIGGER
MEASUREMENT START INPUT AFTER PLL LOCK
(G) MEASUREMENT START SIGNAL (MST)
(H) TEST CYCLE SIGNAL
(I) TEST VECTOR ADDRESS (TBA)
N: INITIAL VALUE N+1 N+2 N+3 N+4 N+3 N+4 N+4 N+3 N+4 N+5
MEMORY ACCESS TIME
(J) TEST VECTOR ADDRESS CONTROL CODE (TBAC)
0x1 0x1 0x1 0x1 0x18 0x1 0x18 0x18 0x1 0x18 0x6
S3=1, S4=1
(N) ALGORITHMIC DATA GENERATION REGISTER CONTROL CODE (ADRC)
EA, EB INPUT OF IMMEDIATE VALUE
CA, CB INPUT OF IMMEDIATE VALUE
MA, MB INPUT OF IMMEDIATE VALUE
MA, MB ADDITION
MA, MB ADDITION
MA, MB ADDITION
MA, MB ADDITION
(O) ALGORITHMIC DATA GENERATION REGISTER CONTROL DATA (ADRD)
0xFF 0x00 0x1 0x1 0x1 0x1
EA, EB INPUT VALUE
CA, CB INPUT VALUE
MA, MB INPUT VALUE
MA, MB ADDITIONAL VALUE
MA, MB ADDITIONAL VALUE
MA, MB ADDITIONAL VALUE
MA, MB ADDITIONAL VALUE
(P) OUTPUTS FROM EFFECTIVE BIT REGISTERS A, B (EBA) (EBB)
0xFF
(Q) OUTPUTS FROM COMPARISON REGISTERS A, B (CRA) (CRB)
0xFF
(R) OUTPUTS FROM MAIN REGISTERS A, B (MRA) (MRB)
0x00 0x01 0xFF 0x00
COINCIDENCE
(S) REGISTER GROUP A COMPARISON COINCIDEN SIGNAL (CCA) (CCB)

FIG. 31

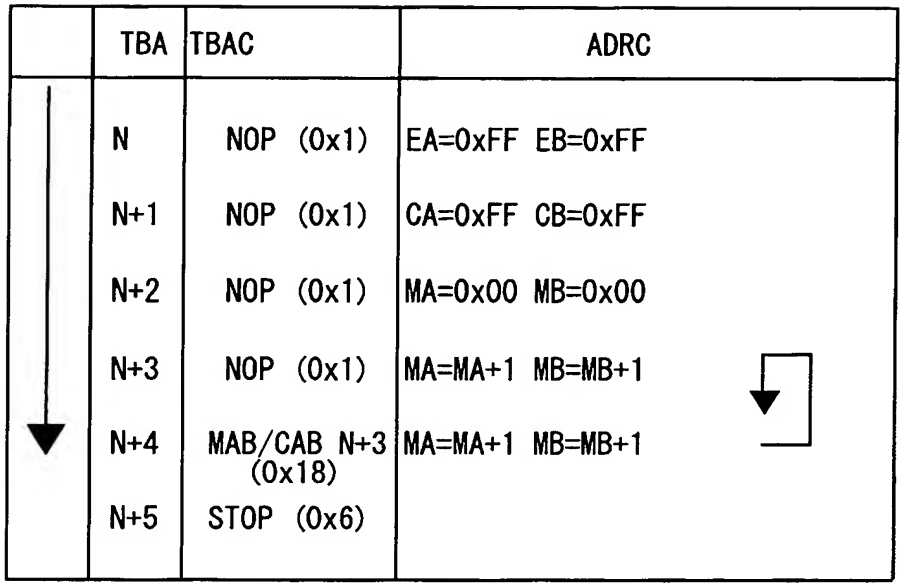

TBA
TBAC
ADRC
N
NOP (0x1)
EA=0xFF EB=0xFF
N+1
NOP (0x1)
CA=0xFF CB=0xFF
N+2
NOP (0x1)
MA=0x00 MB=0x00
N+3
NOP (0x1)
MA=MA+1 MB=MB+1
N+4
MAB/CAB N+3 (0x18)
MA=MA+1 MB=MB+1
N+5
STOP (0x6)

FIG. 32

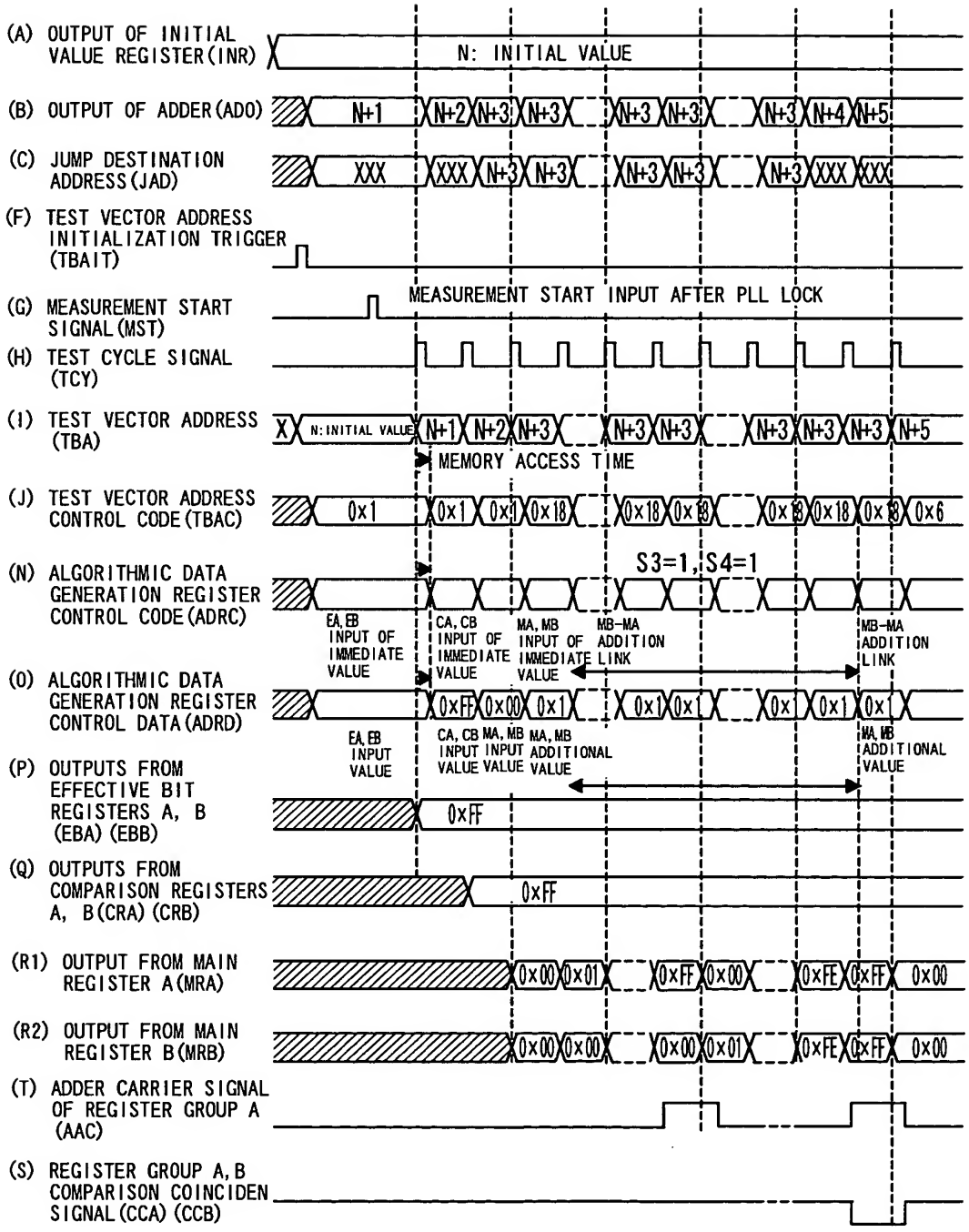

(A) OUTPUT OF INITIAL VALUE REGISTER(INR)
N: INITIAL VALUE
(B) OUTPUT OF ADDER(ADO)
N+1
N+2
N+3
N+4
N+5
(C) JUMP DESTINATION ADDRESS(JAD)
XXX
(F) TEST VECTOR ADDRESS INITIALIZATION TRIGGER (TBAIT)
(G) MEASUREMENT START SIGNAL(MST)
MEASUREMENT START INPUT AFTER PLL LOCK
(H) TEST CYCLE SIGNAL (TCY)
(I) TEST VECTOR ADDRESS (TBA)
N:INITIAL VALUE
MEMORY ACCESS TIME
(J) TEST VECTOR ADDRESS CONTROL CODE(TBAC)
0x1
0x18
0x6
(N) ALGORITHMIC DATA GENERATION REGISTER CONTROL CODE(ADRC)
S3=1, S4=1
EA, EB INPUT OF IMMEDIATE VALUE
CA, CB INPUT OF IMMEDIATE VALUE
MA, MB INPUT OF IMMEDIATE VALUE
MB-MA ADDITION LINK
(O) ALGORITHMIC DATA GENERATION REGISTER CONTROL DATA(ADRD)
0xFF
0x00
EA, EB INPUT VALUE
CA, CB INPUT VALUE
MA, MB INPUT VALUE
MA, MB ADDITIONAL VALUE
(P) OUTPUTS FROM EFFECTIVE BIT REGISTERS A, B (EBA) (EBB)
(Q) OUTPUTS FROM COMPARISON REGISTERS A, B(CRA) (CRB)
(R1) OUTPUT FROM MAIN REGISTER A(MRA)
0x01
(R2) OUTPUT FROM MAIN REGISTER B(MRB)
(T) ADDER CARRIER SIGNAL OF REGISTER GROUP A (AAC)
(S) REGISTER GROUP A, B COMPARISON COINCIDEN SIGNAL(CCA) (CCB)

FIG. 33

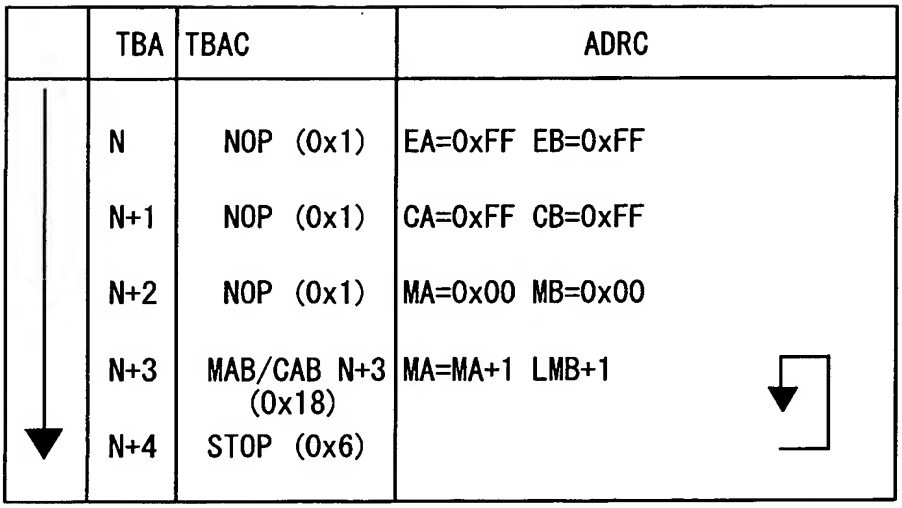

TBA
TBAC
ADRC
N
NOP (0x1)
EA=0xFF EB=0xFF
N+1
NOP (0x1)
CA=0xFF CB=0xFF
N+2
NOP (0x1)
MA=0x00 MB=0x00
N+3
MAB/CAB N+3 (0x18)
MA=MA+1 LMB+1
N+4
STOP (0x6)

FIG. 34

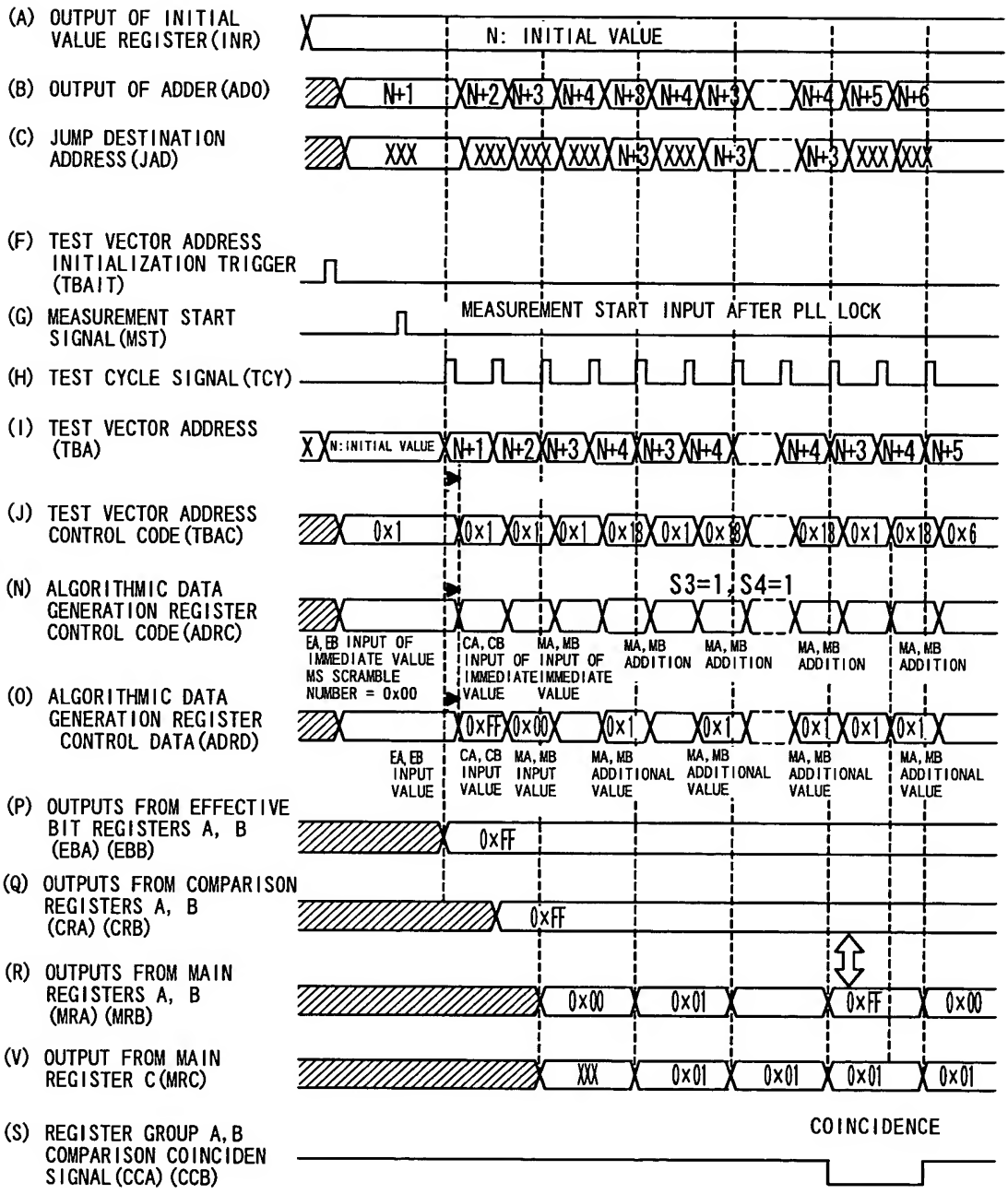

(A) OUTPUT OF INITIAL VALUE REGISTER(INR)
N: INITIAL VALUE
(B) OUTPUT OF ADDER(ADO)
N+1
N+2
N+3
N+4
N+3
N+4
N+3
N+4
N+5
N+6
(C) JUMP DESTINATION ADDRESS(JAD)
XXX
XXX
XXX
XXX
N+3
XXX
N+3
N+3
XXX
XXX
(F) TEST VECTOR ADDRESS INITIALIZATION TRIGGER (TBAIT)
(G) MEASUREMENT START SIGNAL(MST)
MEASUREMENT START INPUT AFTER PLL LOCK
(H) TEST CYCLE SIGNAL(TCY)
(I) TEST VECTOR ADDRESS (TBA)
X
N:INITIAL VALUE
N+1
N+2
N+3
N+4
N+3
N+4
N+4
N+3
N+4
N+5
(J) TEST VECTOR ADDRESS CONTROL CODE(TBAC)
0x1
0x1
0x1
0x1
0x18
0x1
0x18
0x18
0x1
0x18
0x6
(N) ALGORITHMIC DATA GENERATION REGISTER CONTROL CODE(ADRC)
S3=1, S4=1
EA, EB INPUT OF IMMEDIATE VALUE MS SCRAMBLE NUMBER = 0x00
CA, CB INPUT OF IMMEDIATE VALUE
MA, MB INPUT OF IMMEDIATE VALUE
MA, MB ADDITION
MA, MB ADDITION
MA, MB ADDITION
MA, MB ADDITION
(O) ALGORITHMIC DATA GENERATION REGISTER CONTROL DATA(ADRD)
0xFF
0x00
0x1
0x1
0x1
0x1
0x1
EA, EB INPUT VALUE
CA, CB INPUT VALUE
MA, MB INPUT VALUE
MA, MB ADDITIONAL VALUE
MA, MB ADDITIONAL VALUE
MA, MB ADDITIONAL VALUE
MA, MB ADDITIONAL VALUE
(P) OUTPUTS FROM EFFECTIVE BIT REGISTERS A, B (EBA) (EBB)
0xFF
(Q) OUTPUTS FROM COMPARISON REGISTERS A, B (CRA) (CRB)
0xFF
(R) OUTPUTS FROM MAIN REGISTERS A, B (MRA) (MRB)
0x00
0x01
0xFF
0x00
(V) OUTPUT FROM MAIN REGISTER C(MRC)
XXX
0x01
0x01
0x01
0x01
(S) REGISTER GROUP A, B COMPARISON COINCIDEN SIGNAL(CCA) (CCB)
COINCIDENCE

FIG. 35

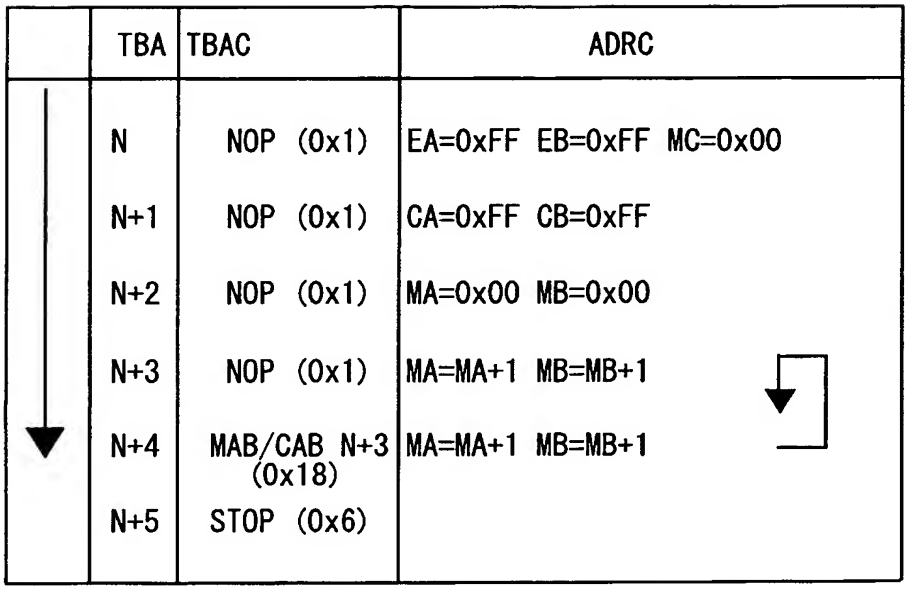

TBA
TBAC
ADRC
N
NOP (0x1)
EA=0xFF EB=0xFF MC=0x00
N+1
NOP (0x1)
CA=0xFF CB=0xFF
N+2
NOP (0x1)
MA=0x00 MB=0x00
N+3
NOP (0x1)
MA=MA+1 MB=MB+1
N+4
MAB/CAB N+3 (0x18)
MA=MA+1 MB=MB+1
N+5
STOP (0x6)

FIG. 36

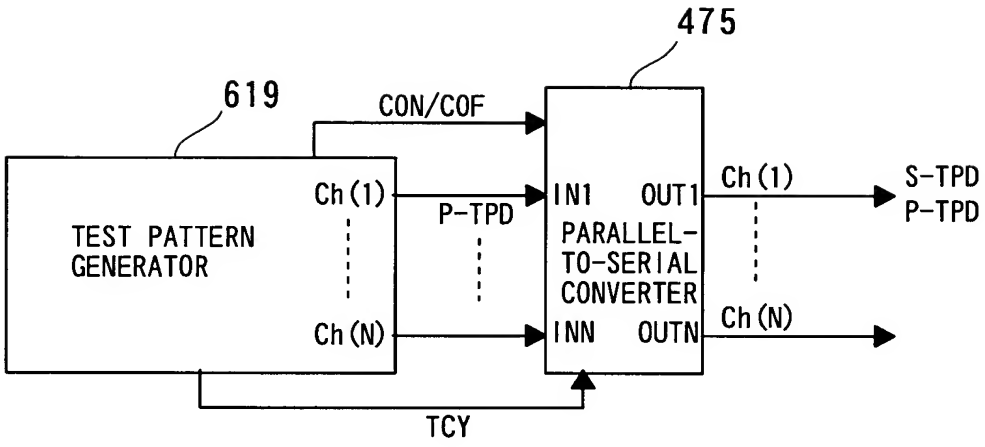

475
619
CON/COF
TEST PATTERN GENERATOR
Ch (1)
Ch (N)
P-TPD
IN1
OUT1
INN
OUTN
PARALLEL-TO-SERIAL CONVERTER
Ch (1)
Ch (N)
S-TPD
P-TPD
TCY

FIG. 37

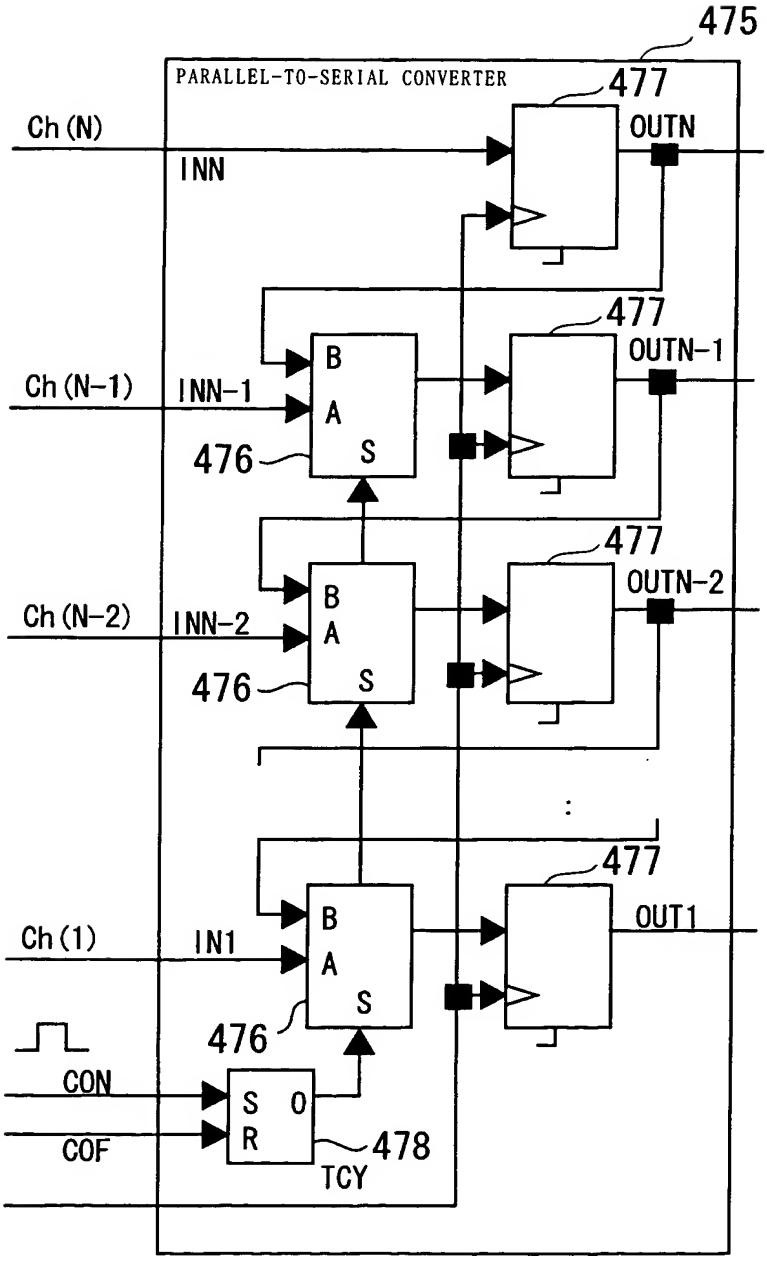

475
PARALLEL-TO-SERIAL CONVERTER
477
OUTN
Ch (N)
INN
477
OUTN-1
Ch (N-1)
INN-1
B
A
S
476
477
OUTN-2
Ch (N-2)
INN-2
B
A
S
476
477
OUT1
Ch (1)
IN1
B
A
S
476
CON
COF
S
R
O
478
TCY

FIG. 38

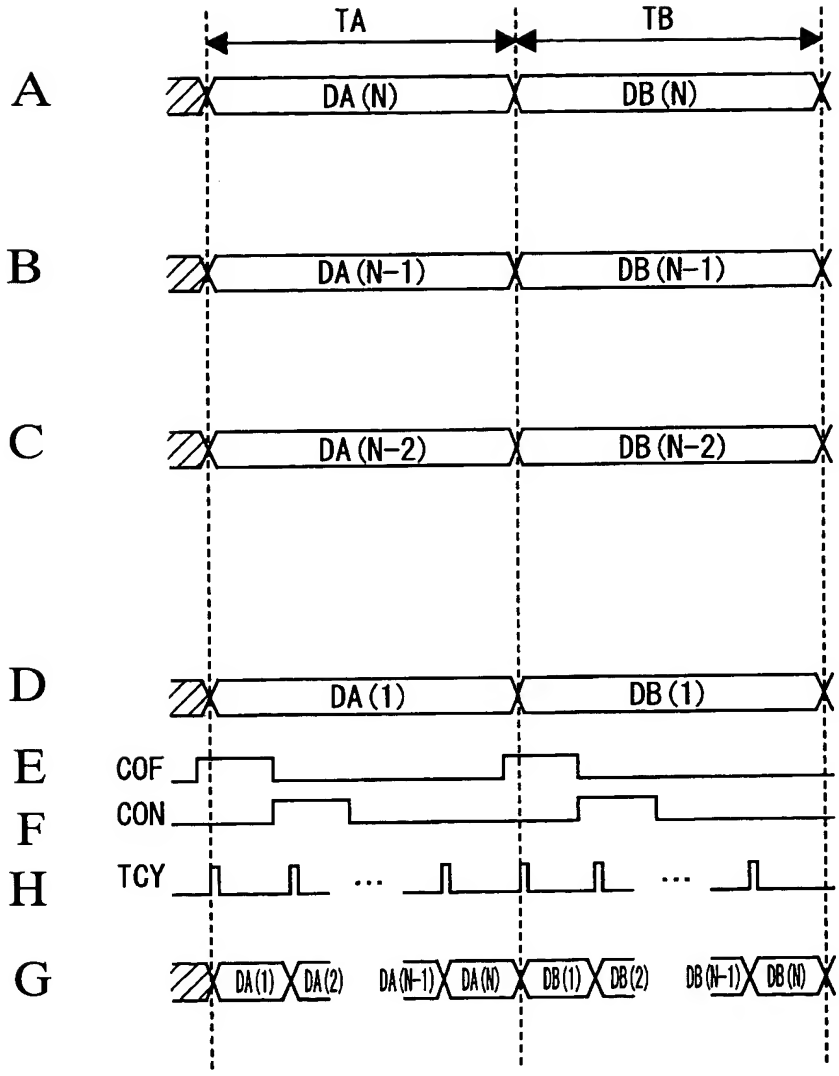

TA
TB
A
DA (N)
DB (N)
B
DA (N-1)
DB (N-1)
C
DA (N-2)
DB (N-2)
D
DA (1)
DB (1)
E
COF
F
CON
H
TCY
G
DA(1)
DA(2)
DA(N-1)
DA(N)
DB(1)
DB(2)
DB(N-1)
DB(N)

FIG. 39

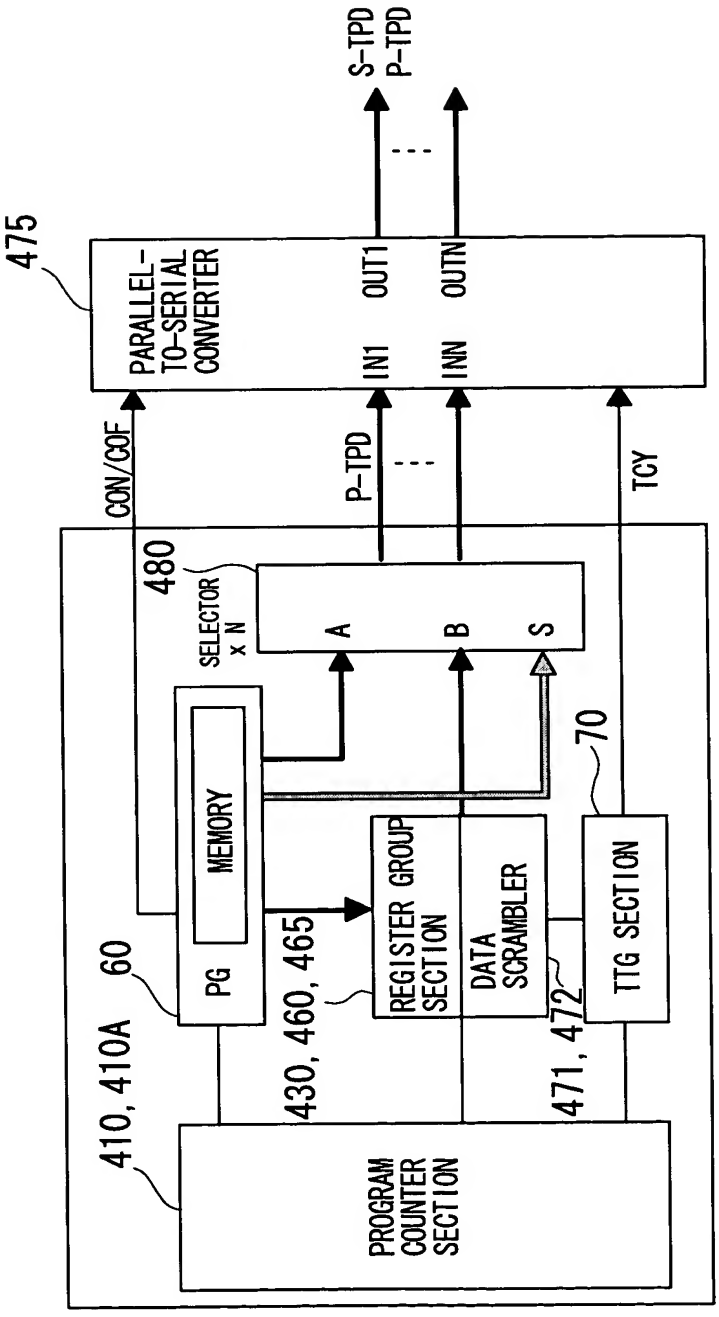

475
PARALLEL-TO-SERIAL CONVERTER
IN1
INN
OUT1
OUTN
S-TPD
P-TPD
CON/COF
P-TPD
TCY
480
SELECTOR x N
A
B
S
MEMORY
PG
60
REGISTER GROUP SECTION
DATA SCRAMBLER
TTG SECTION
70
430, 460, 465
471, 472
410, 410A
PROGRAM COUNTER SECTION

FIG. 40

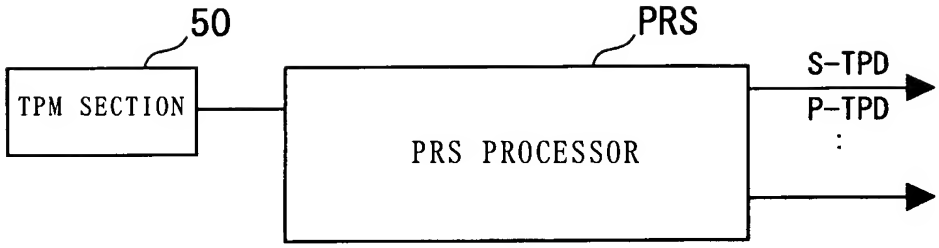


FIG. 41

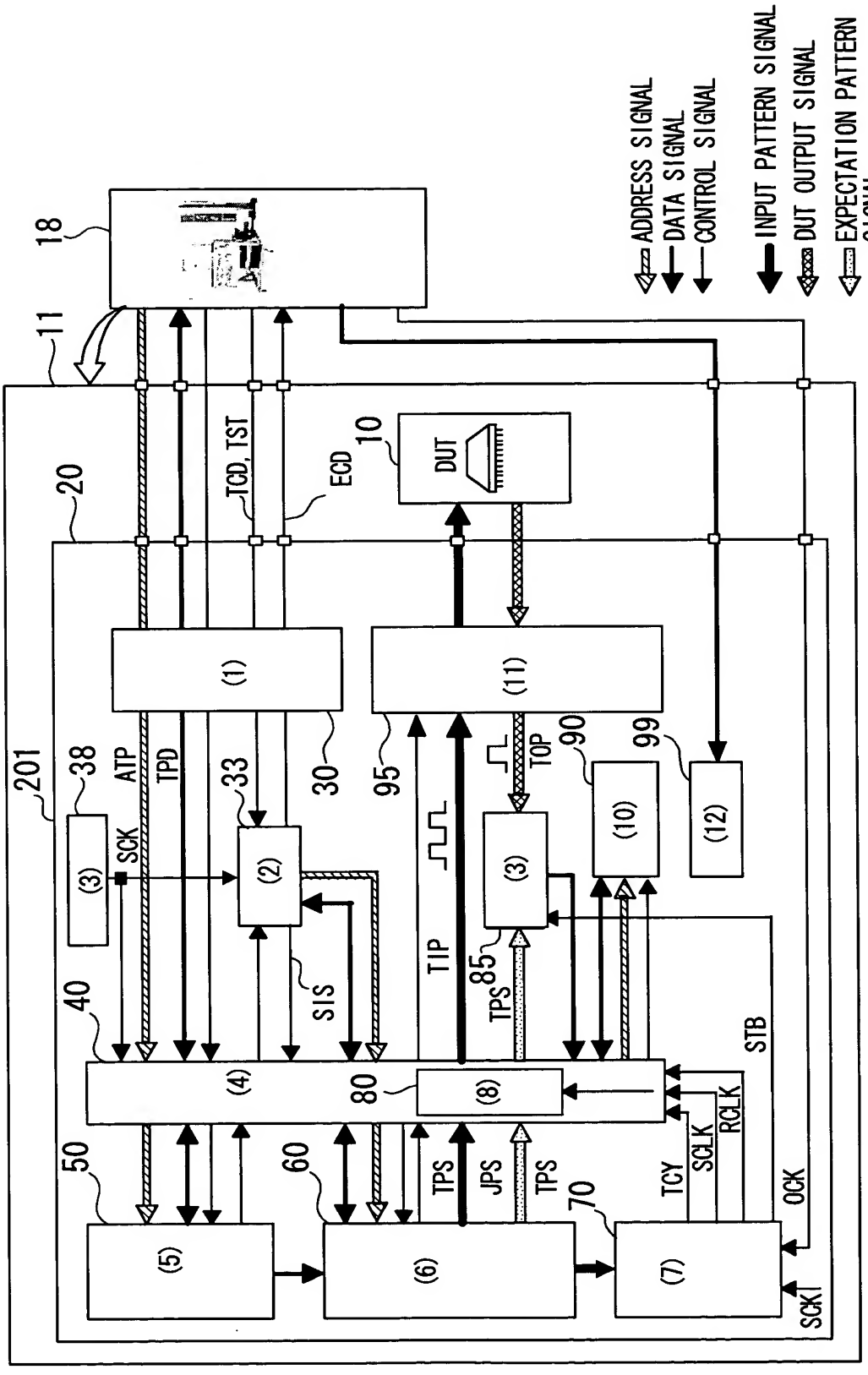

ADDRESS SIGNAL
DATA SIGNAL
CONTROL SIGNAL
INPUT PATTERN SIGNAL
DUT OUTPUT SIGNAL
EXPECTATION PATTERN SIGNAL
18
11
20
201
10
DUT
ECD
TCD, TST
(1)
(11)
38
ATP
TPD
33
30
95
90
99
TOP
(3)
SCK
(2)
(10)
(12)
SIS
TIP
85
TPS
40
(4)
80
(8)
STB
50
60
70
TPS
JPS
TPS
TCY
SCLK
RCLK
OCK
(5)
(6)
(7)
SCK

FIG. 42

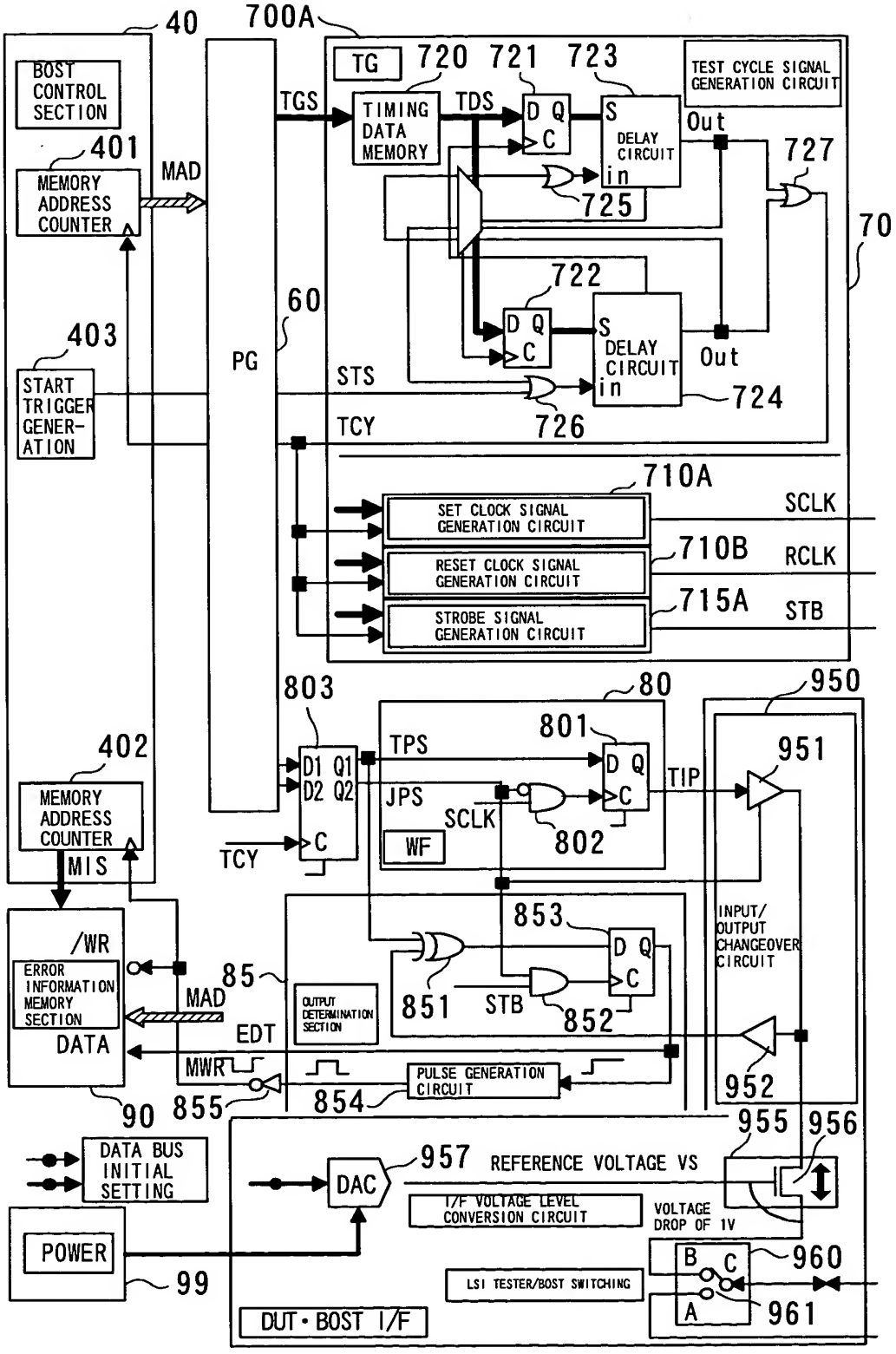

40
700A
BOST CONTROL SECTION
401
MEMORY ADDRESS COUNTER
MAD
403
START TRIGGER GENER-ATION
PG
60
TG
720
721
723
TGS
TIMING DATA MEMORY
TDS
D Q
C
S
DELAY CIRCUIT
in
Out
TEST CYCLE SIGNAL GENERATION CIRCUIT
727
725
722
724
726
STS
TCY
70
710A
SET CLOCK SIGNAL GENERATION CIRCUIT
SCLK
710B
RESET CLOCK SIGNAL GENERATION CIRCUIT
RCLK
715A
STROBE SIGNAL GENERATION CIRCUIT
STB
803
80
950
801
402
MEMORY ADDRESS COUNTER
MIS
D1 Q1
D2 Q2
TPS
JPS
SCLK
WF
802
TIP
951
853
/WR
ERROR INFORMATION MEMORY SECTION
DATA
85
MAD
EDT
OUTPUT DETERMINATION SECTION
851
STB
852
INPUT/ OUTPUT CHANGEOVER CIRCUIT
MWR
PULSE GENERATION CIRCUIT
854
855
952
90
955
956
DATA BUS INITIAL SETTING
DAC
957
REFERENCE VOLTAGE VS
I/F VOLTAGE LEVEL CONVERSION CIRCUIT
VOLTAGE DROP OF 1V
POWER
99
B
C
960
A
961
LSI TESTER/BOST SWITCHING
DUT・BOST I/F

FIG. 43

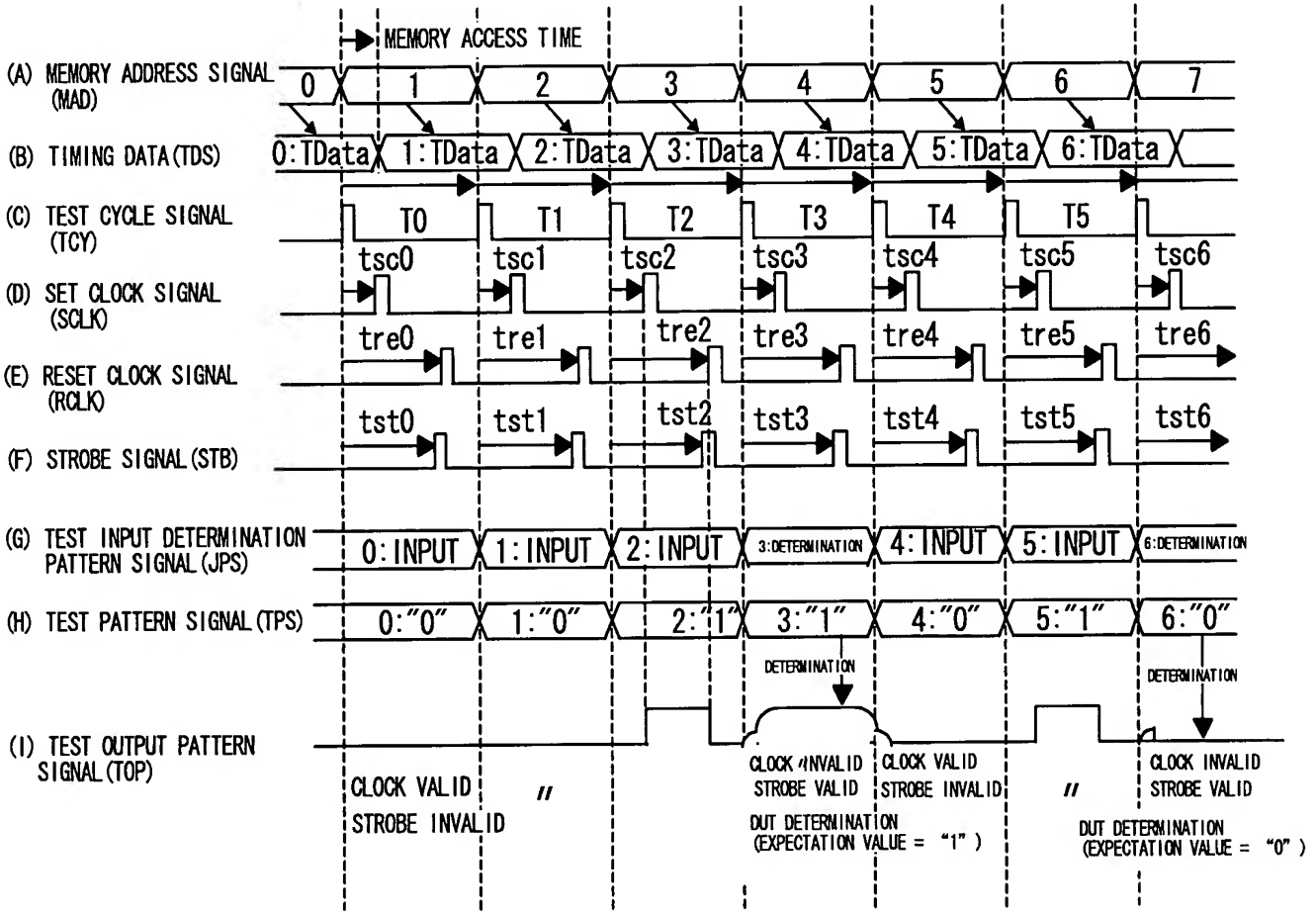

MEMORY ACCESS TIME
(A) MEMORY ADDRESS SIGNAL (MAD)
0
1
2
3
4
5
6
7
(B) TIMING DATA (TDS)
0:TData
1:TData
2:TData
3:TData
4:TData
5:TData
6:TData
(C) TEST CYCLE SIGNAL (TCY)
T0
T1
T2
T3
T4
T5
(D) SET CLOCK SIGNAL (SCLK)
tsc0
tsc1
tsc2
tsc3
tsc4
tsc5
tsc6
(E) RESET CLOCK SIGNAL (RCLK)
tre0
tre1
tre2
tre3
tre4
tre5
tre6
(F) STROBE SIGNAL (STB)
tst0
tst1
tst2
tst3
tst4
tst5
tst6
(G) TEST INPUT DETERMINATION PATTERN SIGNAL (JPS)
0:INPUT
1:INPUT
2:INPUT
3:DETERMINATION
4:INPUT
5:INPUT
6:DETERMINATION
(H) TEST PATTERN SIGNAL (TPS)
0:"0"
1:"0"
2:"1"
3:"1"
4:"0"
5:"1"
6:"0"
DETERMINATION
DETERMINATION
(I) TEST OUTPUT PATTERN SIGNAL (TOP)
CLOCK VALID
STROBE INVALID
//
CLOCK INVALID
STROBE VALID
DUT DETERMINATION
(EXPECTATION VALUE = "1")
CLOCK VALID
STROBE INVALID
//
CLOCK INVALID
STROBE VALID
DUT DETERMINATION
(EXPECTATION VALUE = "0")

FIG. 44

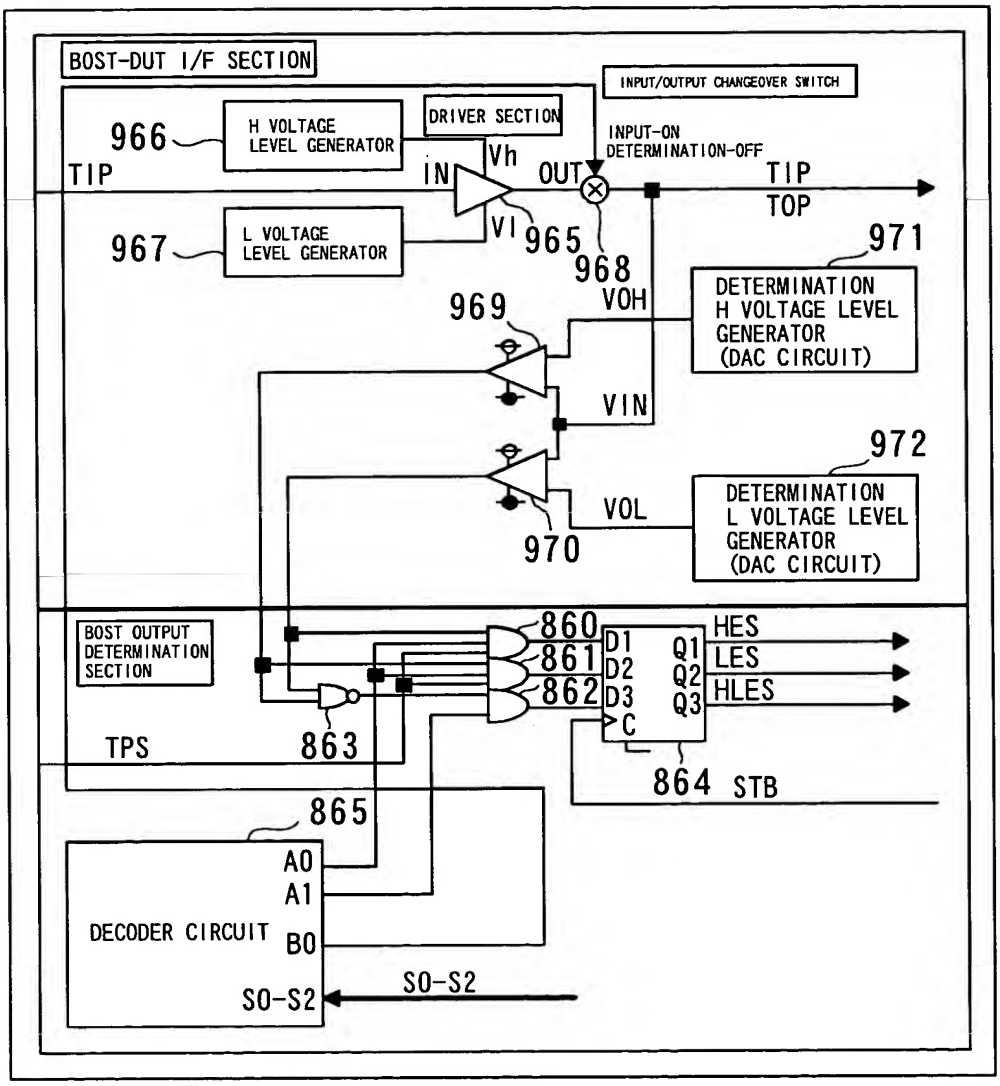

BOST-DUT I/F SECTION
INPUT/OUTPUT CHANGEOVER SWITCH
966
H VOLTAGE LEVEL GENERATOR
DRIVER SECTION
INPUT-ON DETERMINATION-OFF
TIP
IN
Vh
OUT
TIP
TOP
967
L VOLTAGE LEVEL GENERATOR
VI
965
968
971
DETERMINATION H VOLTAGE LEVEL GENERATOR (DAC CIRCUIT)
969
VOH
VIN
972
VOL
DETERMINATION L VOLTAGE LEVEL GENERATOR (DAC CIRCUIT)
970
BOST OUTPUT DETERMINATION SECTION
860
861
862
D1
D2
D3
C
Q1
Q2
Q3
HES
LES
HLES
TPS
863
864
STB
865
A0
A1
DECODER CIRCUIT
B0
S0-S2
S0-S2

FIG. 45

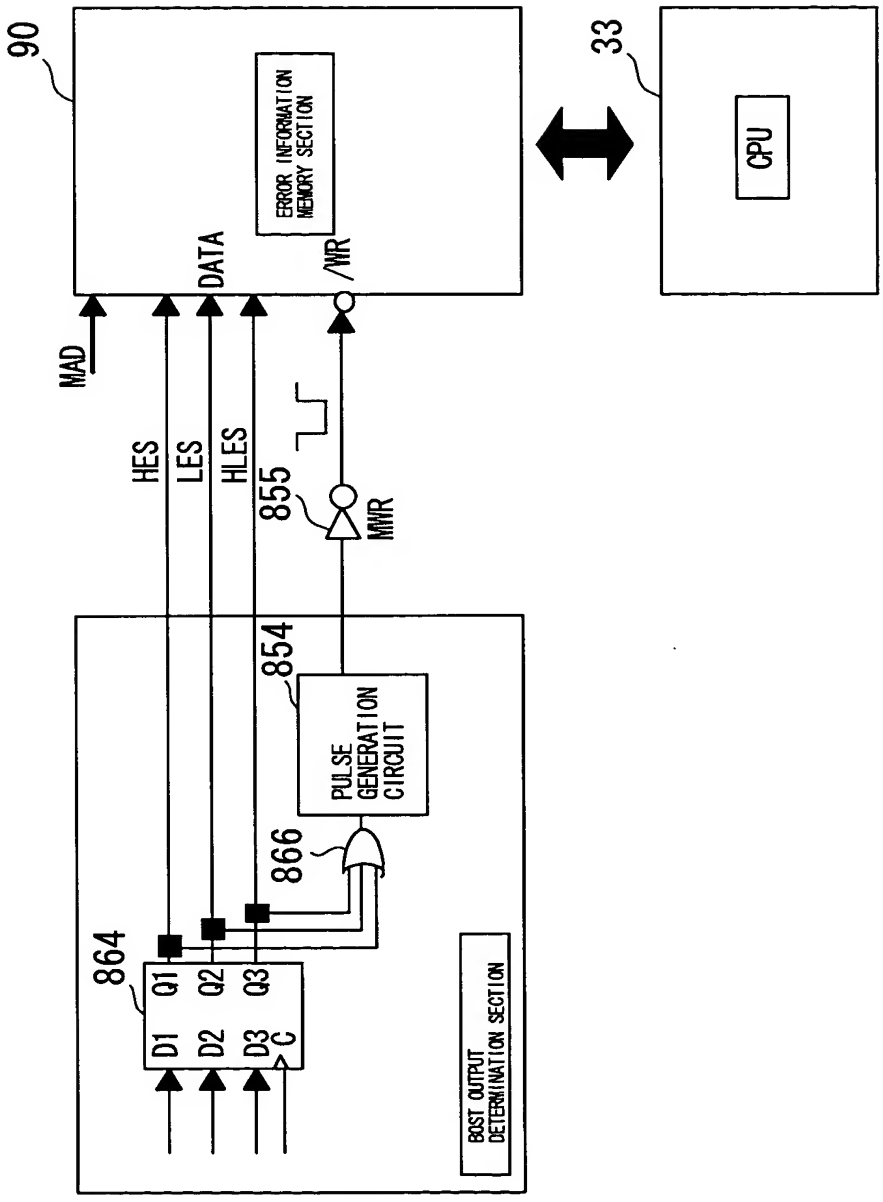

90
33
CPU
ERROR INFORMATION MEMORY SECTION
DATA
/WR
MAD
HES
LES
HLES
855
MWR
854
PULSE GENERATION CIRCUIT
866
864
Q1
Q2
Q3
D1
D2
D3
C
BOST OUTPUT DETERMINATION SECTION

FIG. 46A

FIG. 46B

FIG. 46C

FIG. 46D

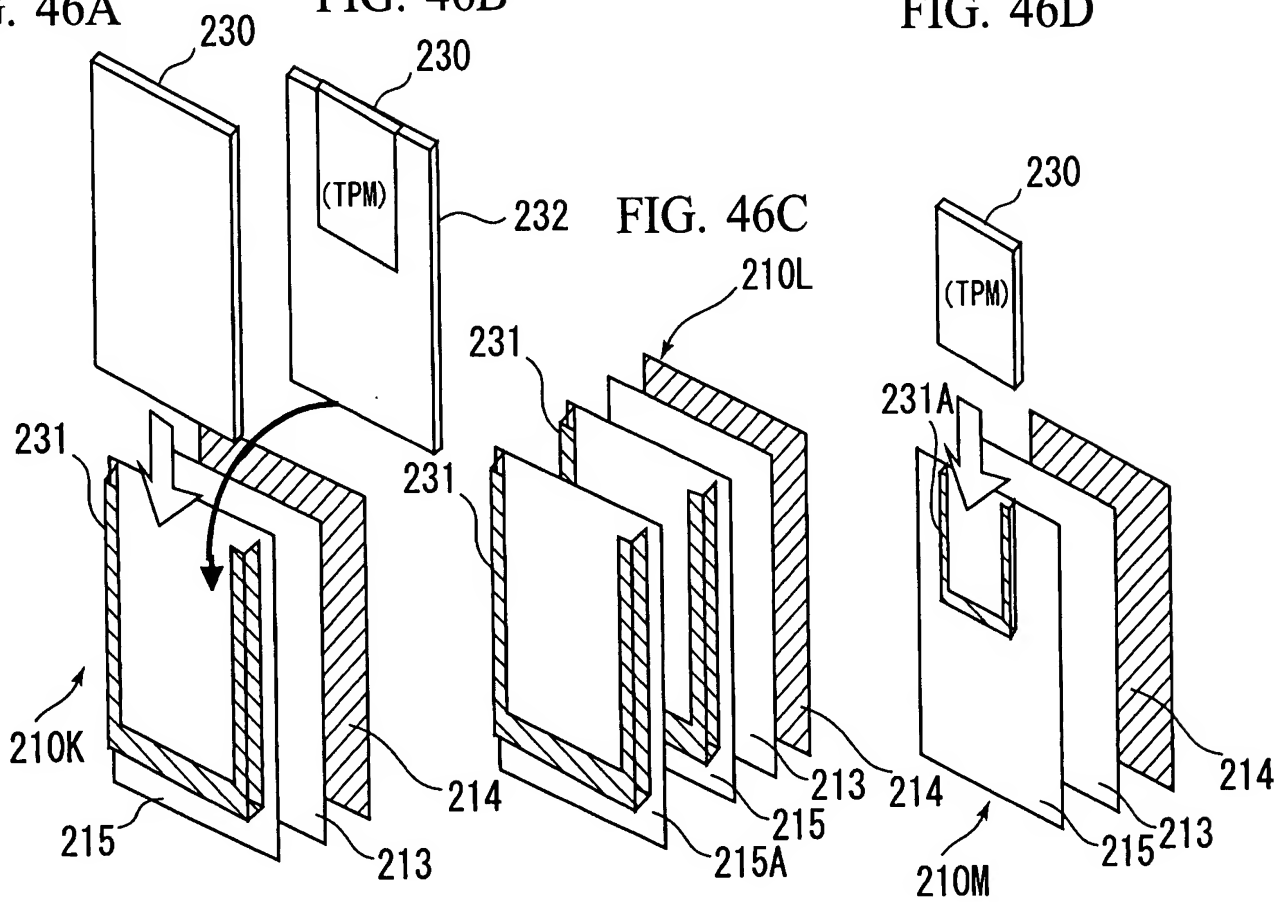


FIG. 47

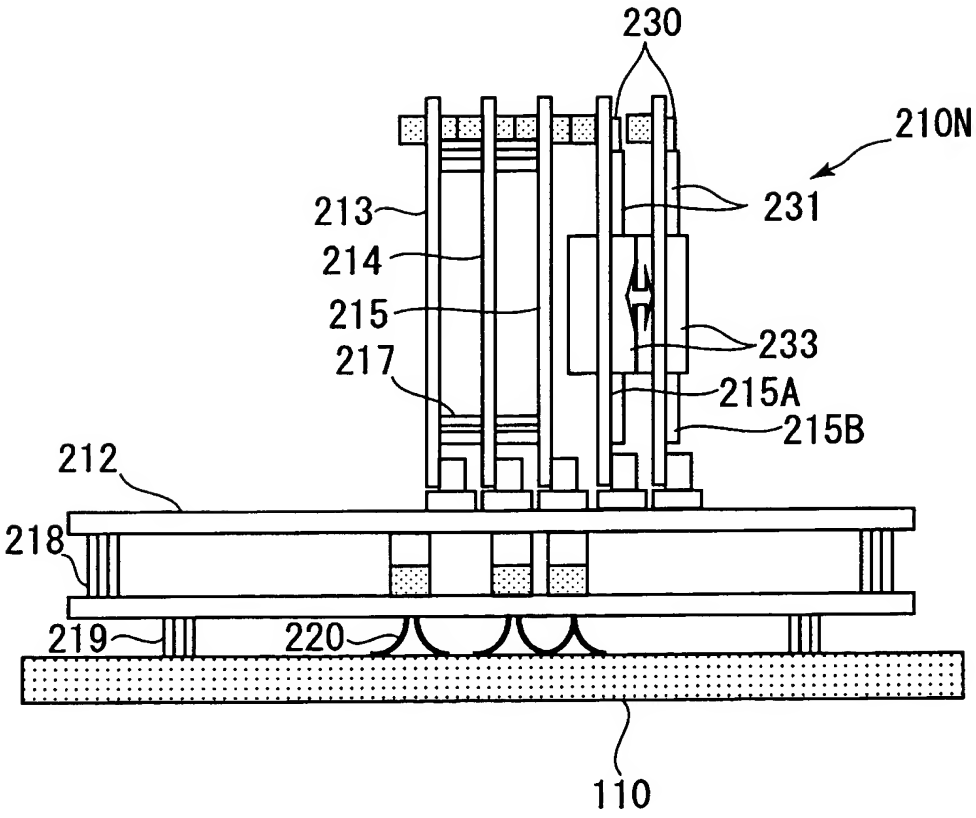


FIG. 48A

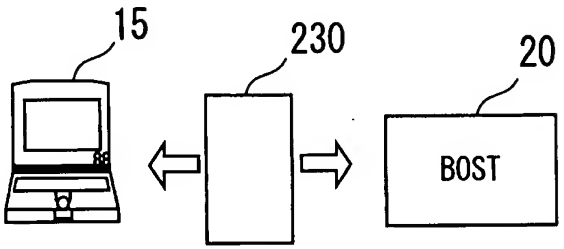


FIG. 48B

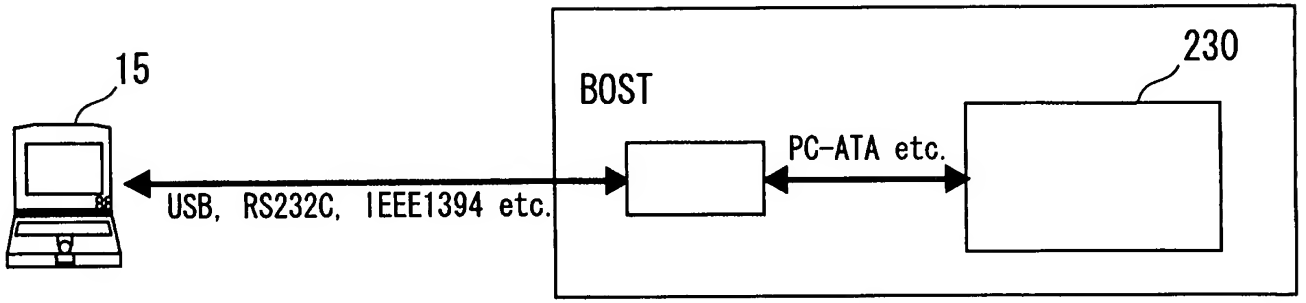


FIG. 49

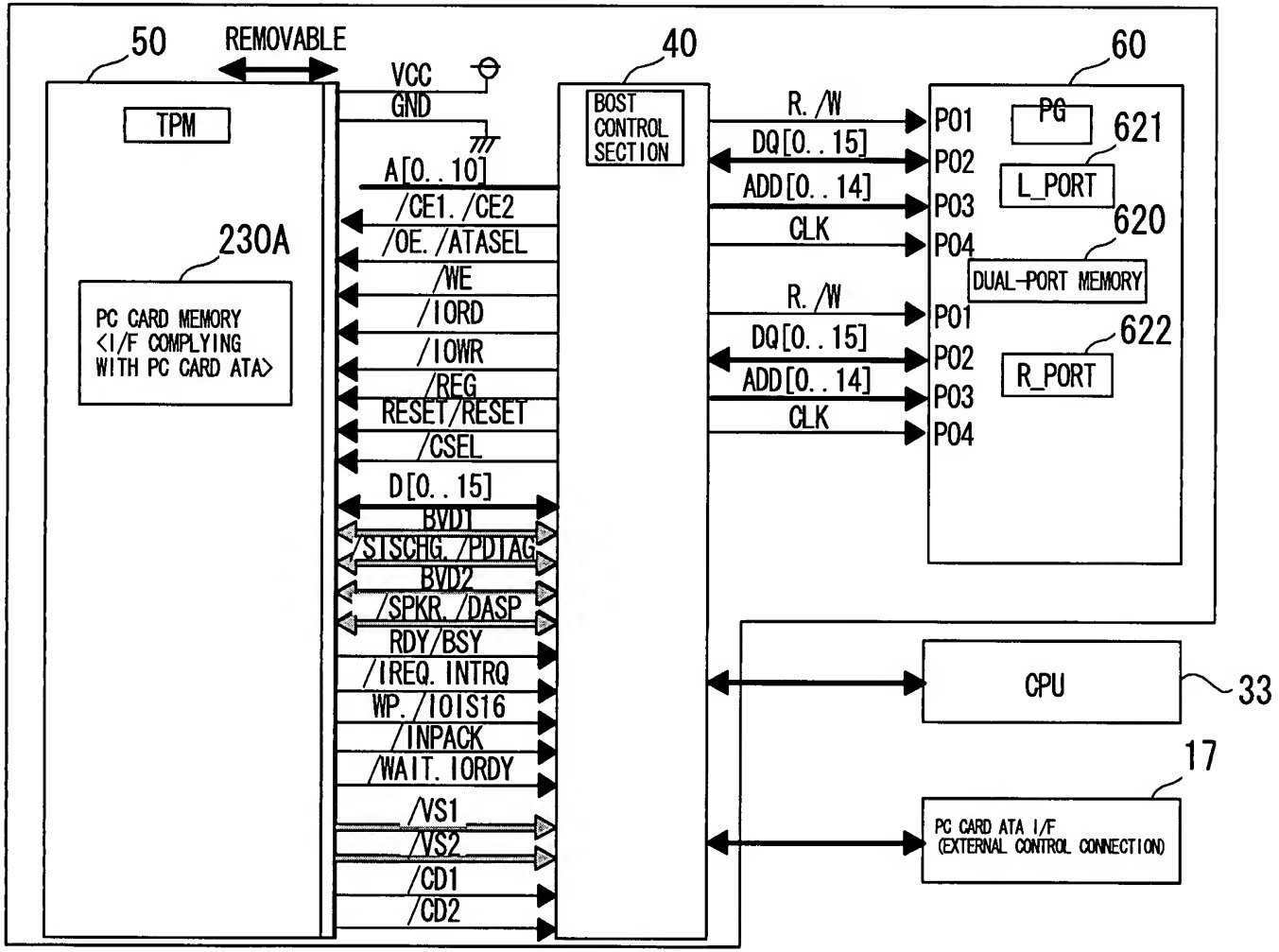

50
REMOVABLE
TPM
230A
PC CARD MEMORY
<I/F COMPLYING
WITH PC CARD ATA>
VCC
GND
A[0..10]
/CE1. /CE2
/OE. /ATASEL
/WE
/IORD
/IOWR
/REG
RESET/RESET
/CSEL
D[0..15]
BVD1
/STSCHG. /PDIAG
BVD2
/SPKR. /DASP
RDY/BSY
/IREQ. INTRQ
WP. /IOIS16
/INPACK
/WAIT. IORDY
/VS1
/VS2
/CD1
/CD2
40
BOST
CONTROL
SECTION
R. /W
DQ[0..15]
ADD[0..14]
CLK
R. /W
DQ[0..15]
ADD[0..14]
CLK
60
P01
P02
P03
P04
P01
P02
P03
P04
PG
621
L_PORT
620
DUAL-PORT MEMORY
622
R_PORT
CPU
33
17
PC CARD ATA I/F
(EXTERNAL CONTROL CONNECTION)

FIG. 50

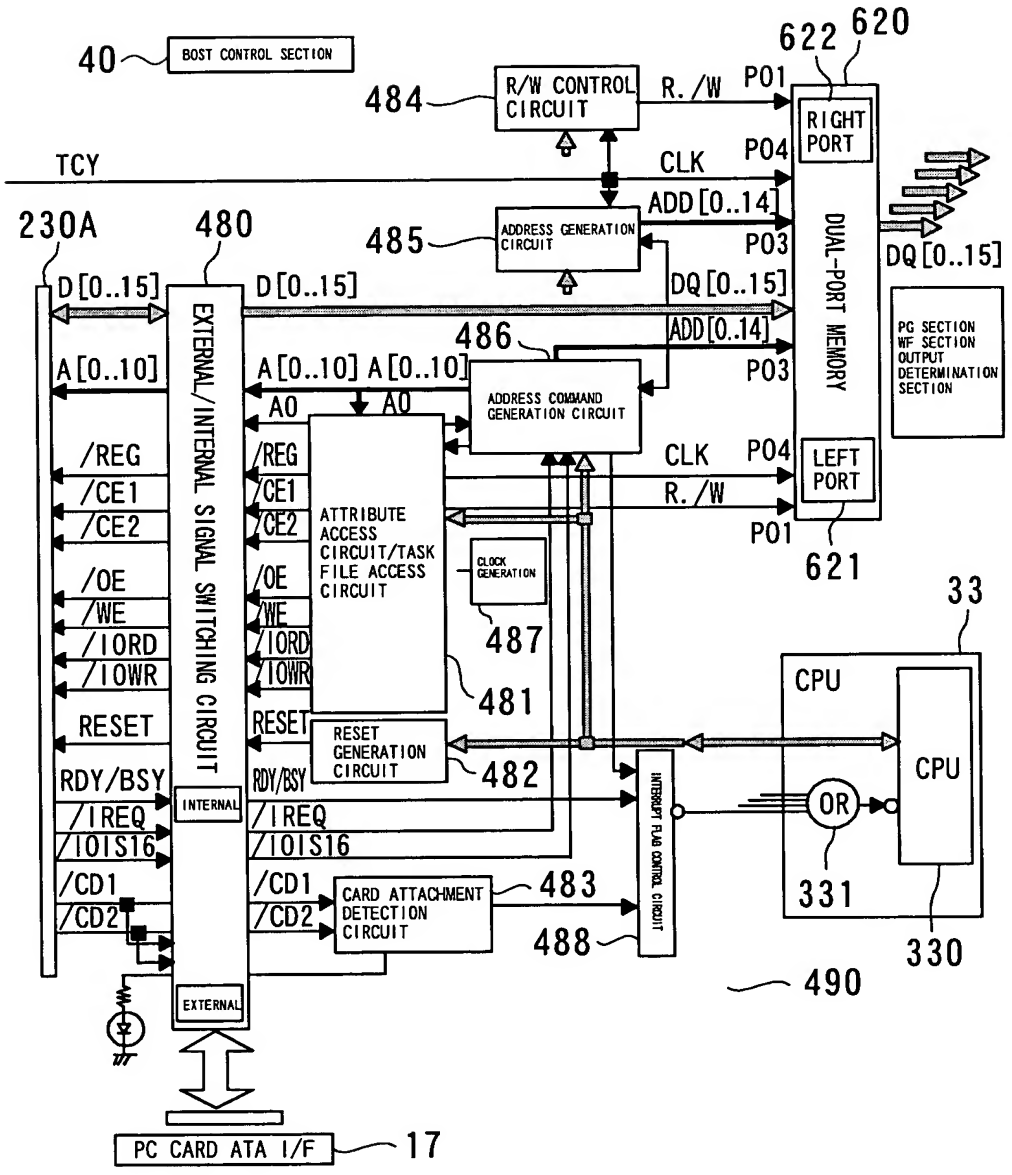

40
BOST CONTROL SECTION
484
R/W CONTROL CIRCUIT
R./W
P01
622
620
RIGHT PORT
TCY
CLK
P04
ADD[0..14]
485
ADDRESS GENERATION CIRCUIT
P03
DUAL-PORT MEMORY
DQ[0..15]
230A
480
D[0..15]
D[0..15]
DQ[0..15]
PG SECTION
WF SECTION
OUTPUT
DETERMINATION
SECTION
ADD[0..14]
486
A[0..10]
A[0..10]
A[0..10]
P03
ADDRESS COMMAND GENERATION CIRCUIT
A0
A0
/REG
/CE1
/CE2
/OE
/WE
/IORD
/IOWR
RESET
RDY/BSY
/IREQ
/IOIS16
/CD1
/CD2
EXTERNAL/INTERNAL SIGNAL SWITCHING CIRCUIT
INTERNAL
EXTERNAL
ATTRIBUTE ACCESS CIRCUIT/TASK FILE ACCESS CIRCUIT
CLOCK GENERATION
487
481
RESET GENERATION CIRCUIT
482
CARD ATTACHMENT DETECTION CIRCUIT
483
488
INTERRUPT FLAG CONTROL CIRCUIT
CLK
P04
R./W
P01
LEFT PORT
621
33
CPU
CPU
OR
331
330
490
PC CARD ATA I/F
17

FIG. 51

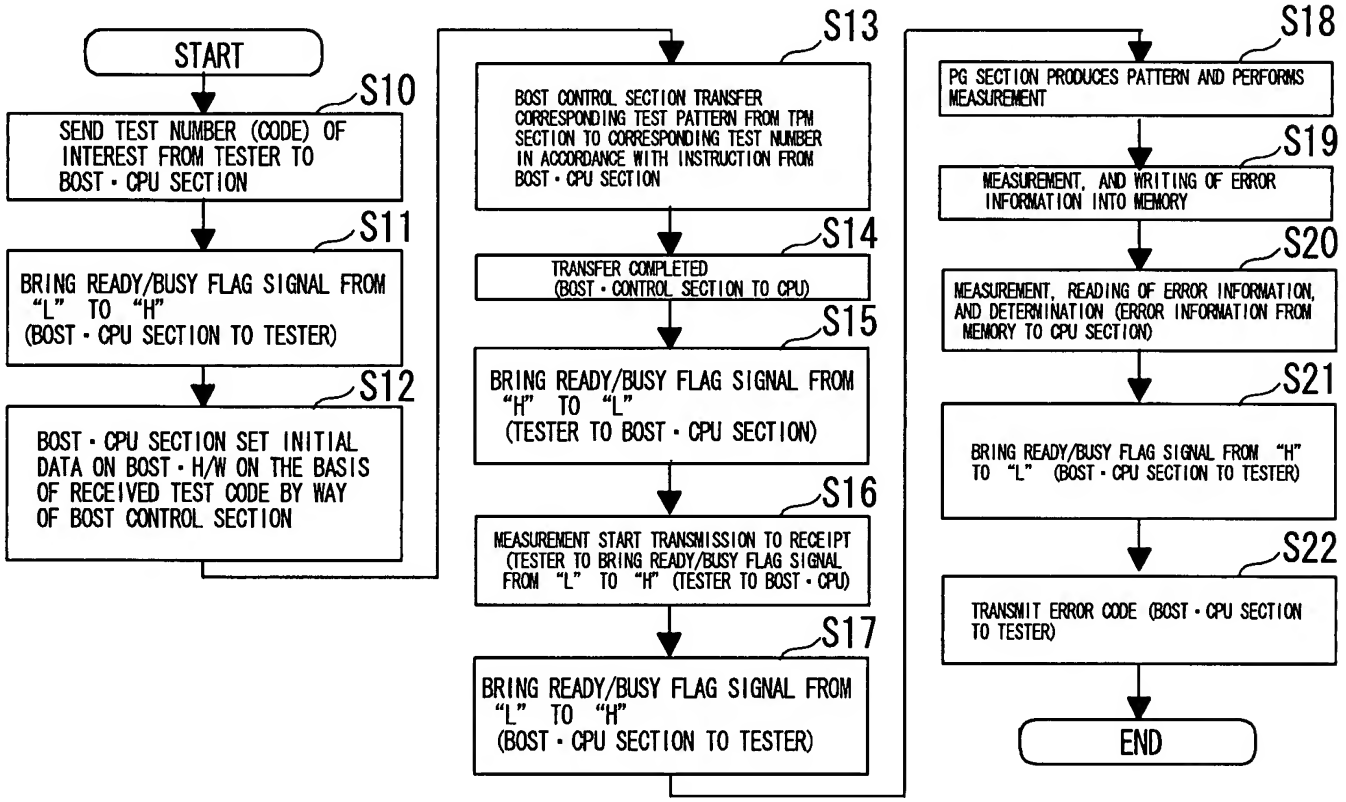

START
S10
SEND TEST NUMBER (CODE) OF INTEREST FROM TESTER TO BOST・CPU SECTION
S11
BRING READY/BUSY FLAG SIGNAL FROM "L" TO "H" (BOST・CPU SECTION TO TESTER)
S12
BOST・CPU SECTION SET INITIAL DATA ON BOST・H/W ON THE BASIS OF RECEIVED TEST CODE BY WAY OF BOST CONTROL SECTION
S13
BOST CONTROL SECTION TRANSFER CORRESPONDING TEST PATTERN FROM TPM SECTION TO CORRESPONDING TEST NUMBER IN ACCORDANCE WITH INSTRUCTION FROM BOST・CPU SECTION
S14
TRANSFER COMPLETED (BOST・CONTROL SECTION TO CPU)
S15
BRING READY/BUSY FLAG SIGNAL FROM "H" TO "L" (TESTER TO BOST・CPU SECTION)
S16
MEASUREMENT START TRANSMISSION TO RECEIPT (TESTER TO BRING READY/BUSY FLAG SIGNAL FROM "L" TO "H" (TESTER TO BOST・CPU)
S17
BRING READY/BUSY FLAG SIGNAL FROM "L" TO "H" (BOST・CPU SECTION TO TESTER)
S18
PG SECTION PRODUCES PATTERN AND PERFORMS MEASUREMENT
S19
MEASUREMENT, AND WRITING OF ERROR INFORMATION INTO MEMORY
S20
MEASUREMENT, READING OF ERROR INFORMATION, AND DETERMINATION (ERROR INFORMATION FROM MEMORY TO CPU SECTION)
S21
BRING READY/BUSY FLAG SIGNAL FROM "H" TO "L" (BOST・CPU SECTION TO TESTER)
S22
TRANSMIT ERROR CODE (BOST・CPU SECTION TO TESTER)
END

FIG. 52

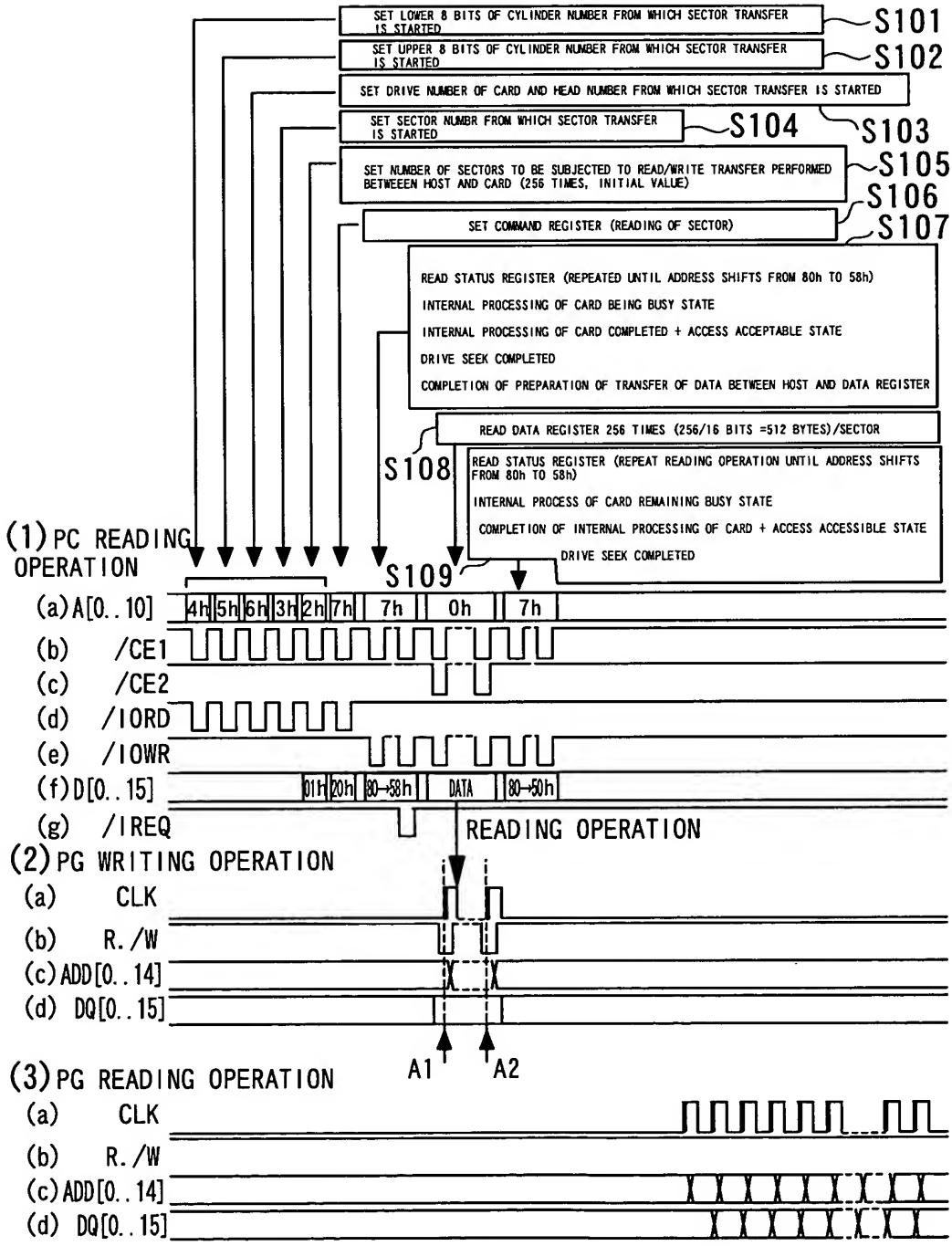

SET LOWER 8 BITS OF CYLINDER NUMBER FROM WHICH SECTOR TRANSFER IS STARTED
S101
SET UPPER 8 BITS OF CYLINDER NUMBER FROM WHICH SECTOR TRANSFER IS STARTED
S102
SET DRIVE NUMBER OF CARD AND HEAD NUMBER FROM WHICH SECTOR TRANSFER IS STARTED
S103
SET SECTOR NUMBR FROM WHICH SECTOR TRANSFER IS STARTED
S104
SET NUMBER OF SECTORS TO BE SUBJECTED TO READ/WRITE TRANSFER PERFORMED BETWEEEN HOST AND CARD (256 TIMES, INITIAL VALUE)
S105
SET COMMAND REGISTER (READING OF SECTOR)
S106
S107
READ STATUS REGISTER (REPEATED UNTIL ADDRESS SHIFTS FROM 80h TO 58h)
INTERNAL PROCESSING OF CARD BEING BUSY STATE
INTERNAL PROCESSING OF CARD COMPLETED + ACCESS ACCEPTABLE STATE
DRIVE SEEK COMPLETED
COMPLETION OF PREPARATION OF TRANSFER OF DATA BETWEEN HOST AND DATA REGISTER
READ DATA REGISTER 256 TIMES (256/16 BITS =512 BYTES)/SECTOR
S108
READ STATUS REGISTER (REPEAT READING OPERATION UNTIL ADDRESS SHIFTS FROM 80h TO 58h)
INTERNAL PROCESS OF CARD REMAINING BUSY STATE
COMPLETION OF INTERNAL PROCESSING OF CARD + ACCESS ACCESSIBLE STATE
DRIVE SEEK COMPLETED
S109
(1) PC READING OPERATION
(a) A[0..10]
4h 5h 6h 3h 2h 7h 7h 0h 7h
(b) /CE1
(c) /CE2
(d) /IORD
(e) /IOWR
(f) D[0..15]
01H 20h 80→58h DATA 80→50h
(g) /IREQ
READING OPERATION
(2) PG WRITING OPERATION
(a) CLK
(b) R./W
(c) ADD[0..14]
(d) DQ[0..15]
A1
A2
(3) PG READING OPERATION
(a) CLK
(b) R./W
(c) ADD[0..14]
(d) DQ[0..15]

FIG. 53

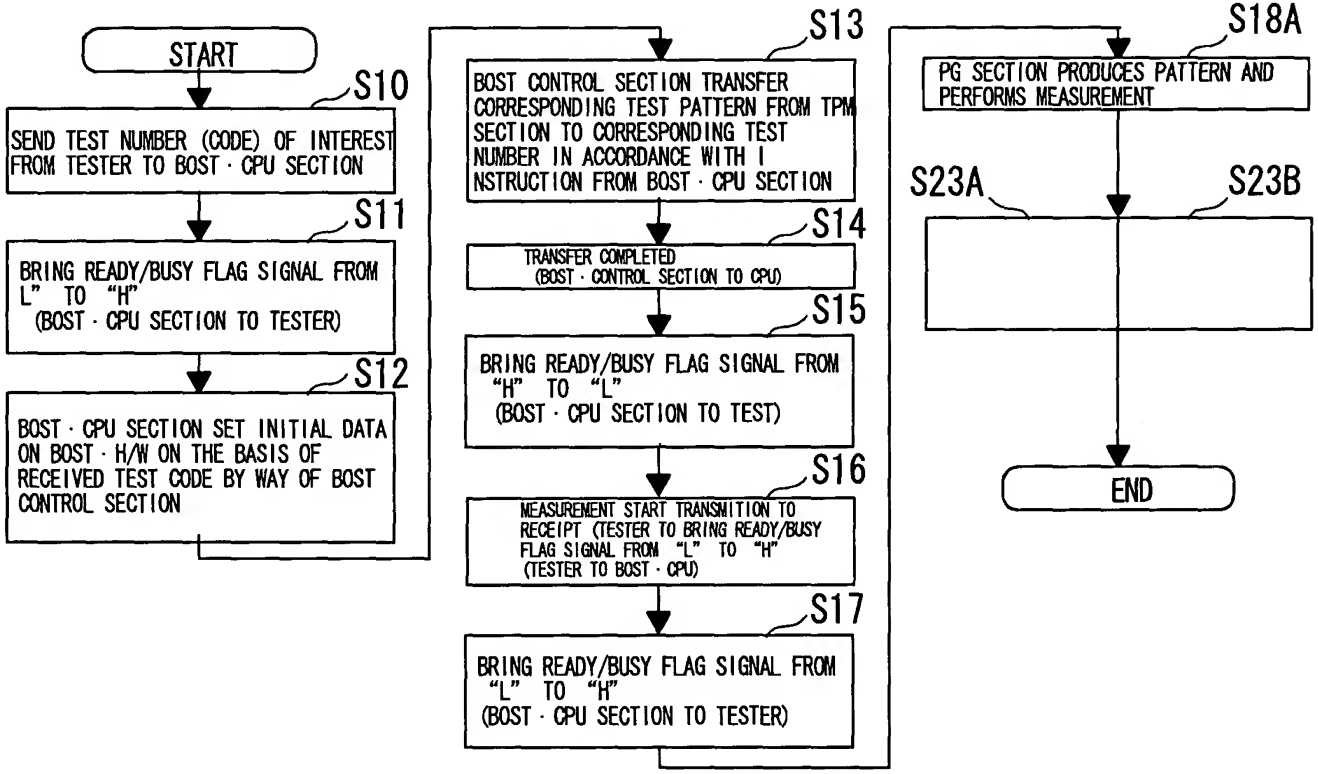

START
S10
SEND TEST NUMBER (CODE) OF INTEREST FROM TESTER TO BOST · CPU SECTION
S11
BRING READY/BUSY FLAG SIGNAL FROM L" TO "H" (BOST · CPU SECTION TO TESTER)
S12
BOST · CPU SECTION SET INITIAL DATA ON BOST · H/W ON THE BASIS OF RECEIVED TEST CODE BY WAY OF BOST CONTROL SECTION
S13
BOST CONTROL SECTION TRANSFER CORRESPONDING TEST PATTERN FROM TPM SECTION TO CORRESPONDING TEST NUMBER IN ACCORDANCE WITH I NSTRUCTION FROM BOST · CPU SECTION
S14
TRANSFER COMPLETED (BOST · CONTROL SECTION TO CPU)
S15
BRING READY/BUSY FLAG SIGNAL FROM "H" TO "L" (BOST · CPU SECTION TO TEST)
S16
MEASUREMENT START TRANSMITTION TO RECEIPT (TESTER TO BRING READY/BUSY FLAG SIGNAL FROM "L" TO "H" (TESTER TO BOST · CPU)
S17
BRING READY/BUSY FLAG SIGNAL FROM "L" TO "H" (BOST · CPU SECTION TO TESTER)
S18A
PG SECTION PRODUCES PATTERN AND PERFORMS MEASUREMENT
S23A
S23B
END

FIG. 54

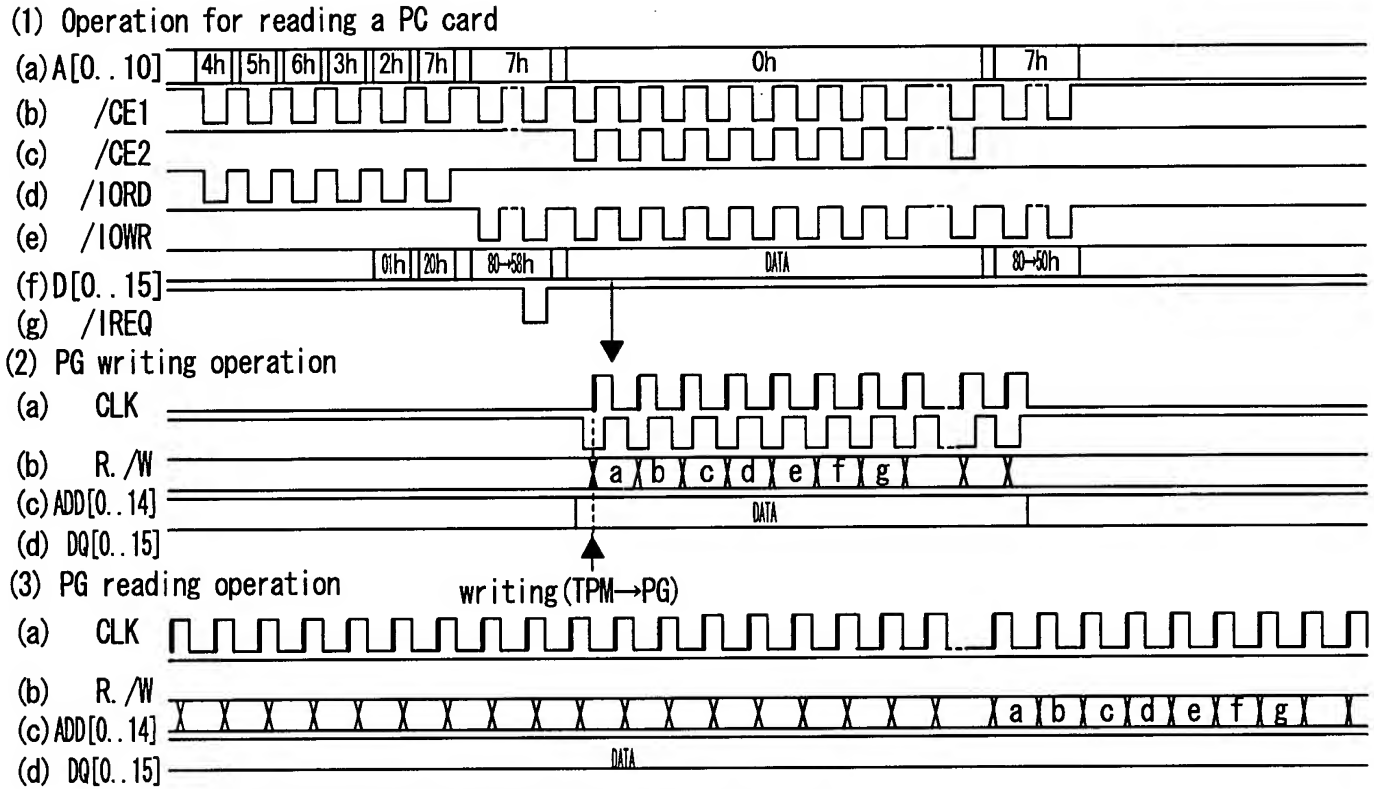
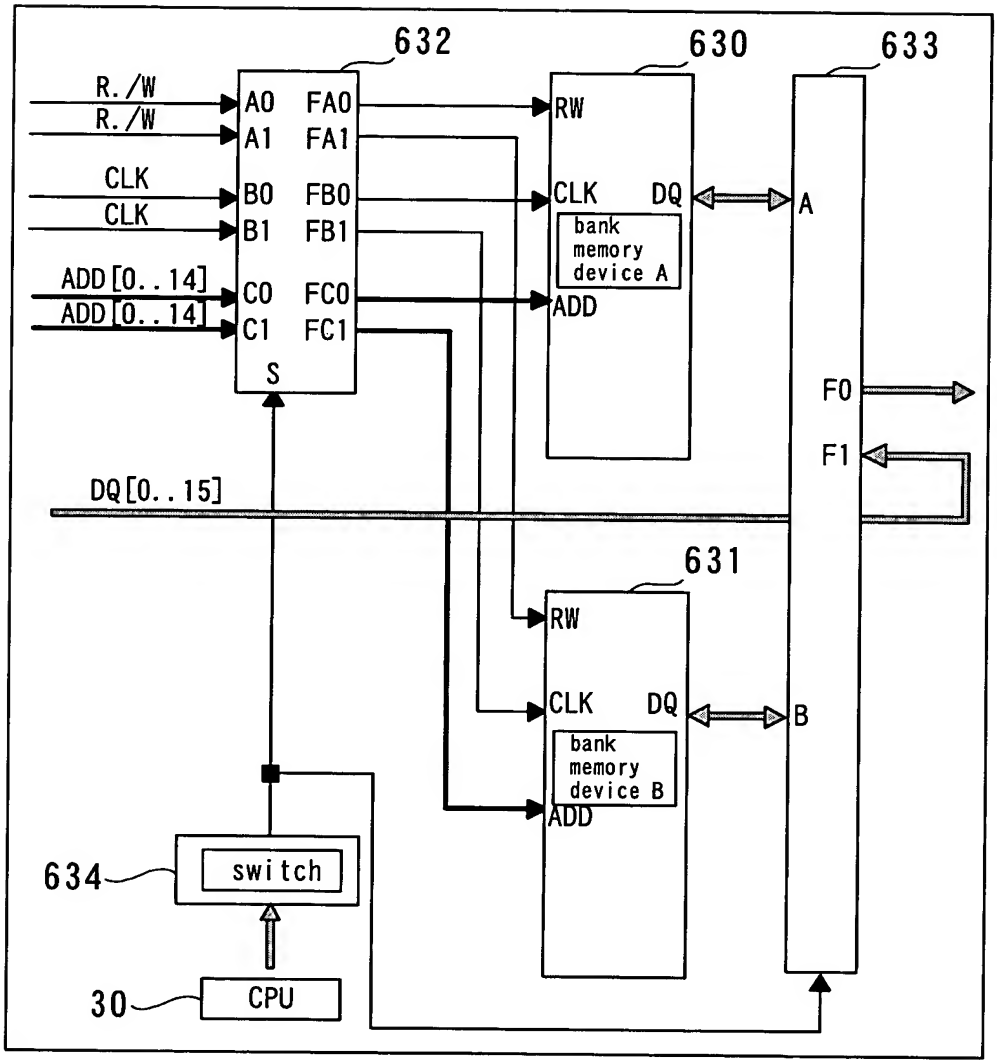

(1) Operation for reading a PC card
(a) A[0..10]
4h
5h
6h
3h
2h
7h
7h
0h
7h
(b) /CE1
(c) /CE2
(d) /IORD
(e) /IOWR
01h
20h
80→58h
DATA
80→50h
(f) D[0..15]
(g) /IREQ
(2) PG writing operation
(a) CLK
(b) R./W
a
b
c
d
e
f
g
(c) ADD[0..14]
DATA
(d) DQ[0..15]
(3) PG reading operation
writing(TPM→PG)
(a) CLK
(b) R./W
a
b
c
d
e
f
g
(c) ADD[0..14]
DATA
(d) DQ[0..15]

FIG. 55


632
630
633
R./W
R./W
CLK
CLK
ADD[0..14]
ADD[0..14]
A0
A1
B0
B1
C0
C1
S
FA0
FA1
FB0
FB1
FC0
FC1
RW
CLK
DQ
bank memory device A
ADD
A
F0
F1
DQ[0..15]
631
RW
CLK
DQ
bank memory device B
ADD
B
634
switch
30
CPU